ADJACENT MULTI-BIT ERROR DETECTING AND CORRECTING CODES FOR MEDICAL APPLICATIONS

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ABSTRACT

In medical applications while transmission of images errors occurs especially in telemedicine. Due to errors there is a possibility of wrong diagnosis while treatment. The aim of this paper is to develop Adjacent Multi-Bit Error Detecting and Correcting Codes with minimum redundant bits and maximum code rate. Also coding techniques like matrix codes are used to maintain effective transmission. The codes are represented in verilog hardware description language and simulated in the Tool Xilinx ISE 14.5 for XC7Z020-1CLG484 FPGA. The implemented code is more effective as compared to matrix codes, it reduces bit overhead at least by 5.5% to 46.96% and coding rate increased at least by 16.74% to 23.85%.

KEYWORDS

Adjacent Multi-Bit Errors, Code Rate, Telemedicine, Redundant Bits, Error Detecting and Correcting Codes.

1. INTRODUCTION

Telemedicine plays a major role in medical applications. It provides remote clinical services to patients through make use of information technology and electronic communication. Telemedicine is the practice of medicine that uses technology to provide care to patients who are located far away. To provide care to a patient in a remote location, a physician at one place uses a telecommunications infrastructure. With telemedicine, you can communicate with a healthcare provider in real time via video, web portals, and email about symptoms, medical difficulties and more. Several examples of telemedicine are

1. Digital transmission of diagnostic imaging,
2. Distant clinical diagnosis and estimation and
3. Video conferences with experts.

When the patients details are communicated among doctors by online, due to errors introduced during transmission, the affected parts of the image may be modified.

There exist two cases:

[1] If the affected part of image gets enlarged due to errors in transmission, there is a possibility of wrong diagnosis stating that the patient need to be operated.
[2] If the affected part of images gets compressed due to errors in transmission, there is a possibility of wrong diagnosis stating that it might decrease over a period of time and there is no need for any surgery which might make the patient to suffer.

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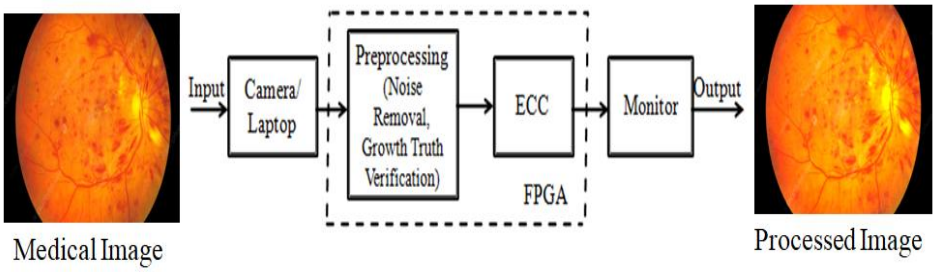

Figure1. Diagram of implementation methodology

From figure1 input is considered as a diabetic retinopathy image. They are pre-processed to remove the noise in image and then they are verified with growth truth images. Then the code implementation on FPGA is used for detection and correction of errors during transmission. Finally, the results are viewed on output device i.e., on monitor.

Usually as the information is sent over a noisy channel, it undergoes distortion. Hence, there is a need for coding which offers efficient transmission, error detection and correction.

Coding is a technique by which the characteristics of information are tailored so as to make ready for the intended application. Coding schemes depend on safety requirement, transmission medium, tolerance level and need for standardization.

Decoding is a technique of restoring source information from the encoded information received. It can be more complicated as compared to coding if one has little knowledge of various coding schemes.

Errors are grouped as in figure2. Among these this paper focuses on adjacent error correction.

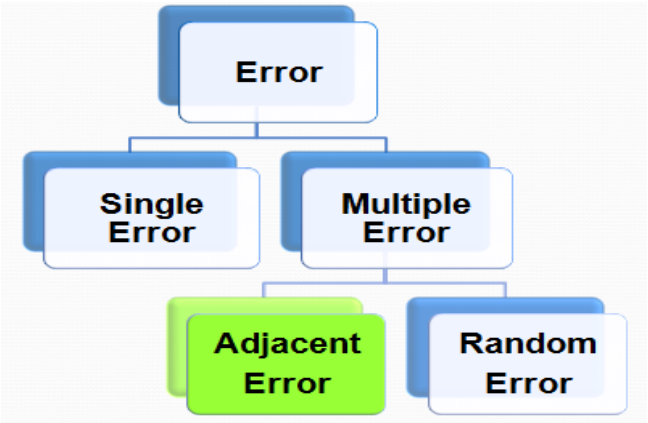

Figure2. Error classification

In this paper, Section II gives a summary of current codes and Section III discusses about new codes. The results are discussed in Section IV, and then paper is finished.

2. EXISTING MATRIX CODES

The existing system presents the Decimal and Modified Decimal Matrix Code [4][5]. DMC uses a decimal algorithm to obtain decimal integer addition and subtraction to detect the errors. The number of error detection capability and memory reliability is increased by using decimal algorithm. Figure3. depicts entire process.

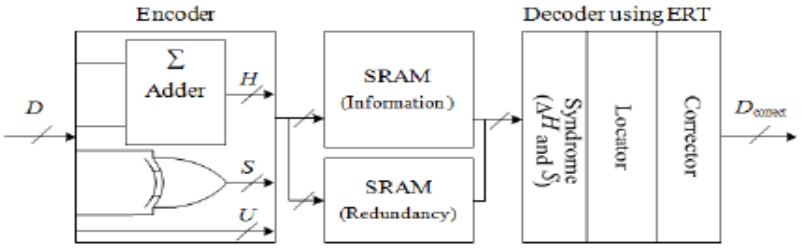

Figure3. Block diagram of DMC

The data bits D are transmitted to a DMC encoder, which uses a decimal adder to compute horizontal redundant bits H and an exclusive-OR operation to compute vertical redundant bits V. Register U stores the encoded data as well as a copy of the information data.

By using encoder reuse technique (ERT), the area of DMC can be minimized. For parity bits, the H bits and V bits were used [8].

$$H1H0 = D2 + D0 \quad (1)$$
$$H3H2 = D3 + D1 \quad (2)$$
$$H5H4 = D6 + D4 \quad (3)$$
$$H7H6 = D1 + D5 \quad (4)$$

And

$$V0 = D0 \oplus D4 \quad (5)$$

.
.

$$V3 = D3 \oplus D7$$

Also

$$U = D \quad (6)$$

During write operation, the data stored in information and redundancy SRAM [1][2]. During read operation, syndrome bits are used to correct the multiple bit upsets if occurs i.e., by utilizing a process such as

First, memory is read for the redundant bits H5H4H3H2H1H0’ and V0’- V3’ formed from data bits. Second, the horizontal (ΔH4...H0) and vertical (S3...S0) syndrome bits can be computed as below.

$$\Delta H4H3H2H1H0 = H4H3H2H1H0' - H4H3H2H1H \quad (7)$$
$$S0 = V0' \oplus V0 \quad (8)$$

.
.

$$S3 = V3' \oplus V3$$

When ΔH and S would both be zero, the information read is identical to the original information bits, with no errors. The induced errors are observed and located when ΔH and S are nonzero [7] and the errors can be computed by

$$Dcorrect = D \oplus S \qquad (9)$$

The Syndrome, locator and corrector are the three sub modules of the DMC decoder. Each one performs a specific purpose in the decoding process. To obtain the syndrome bits ΔHand S, the received H and V bits are computed first and then compared to the initial set of redundant bits in the decoding process.

Here this 8-bit data is for DMC decoder in the same way for 16-bit, 32-bit and 64 bit of data can be organized [6].

Similarly, for MDMC the adjustment is completed by changing the H-bits to include upper and lower half data bits i.e.,

$$H2H1H0 = D3D2 + D1D0 \qquad (10)$$
$$H5H4H3 = D7D6 + D5D4 \qquad (11)$$

This means the horizontal parity bits are reduced by 2.

3. PROPOSED MATRIX CODE

The basic mechanism of encoding that is used is as depicted in figure4 i.e., Consider an 8-bit data being arranged. Here V [3...0] are the vertical encoded parity bits and H [1...0] are the half diagonal parity bits.

D7	D6	D5	D4	H2
D3	D2	D1	D0	H1
V3	V2	V1	V0	H0

Figure4. Encoding Mechanism

The vertical parity bits are calculated as

$$V0 = D0 \oplus D4$$
$$V1 = D1 \oplus D5$$
$$V2 = D2 \oplus D6$$
$$V3 = D3 \oplus D7$$

The half diagonal parity bits are calculated as

$$H0 = D2 \oplus D0$$
$$H1 = D7 \oplus D6 \oplus D1 \oplus D0$$
$$H2 = D7 \oplus D6 \oplus D5 \oplus D4$$

The decoding mechanism is same as that of DMC and MDMC except that the ΔH is calculated from modulo-2 addition. Also the error is detected only if ΔH and S are nonzero numbers.

4. RESULTS AND DISCUSSION

For modeling verilog hardware description language was utilized and the Codes are functionally tested in Xilinx ISE 14.5 Tool for XC7Z020-1CLG484 FPGA.

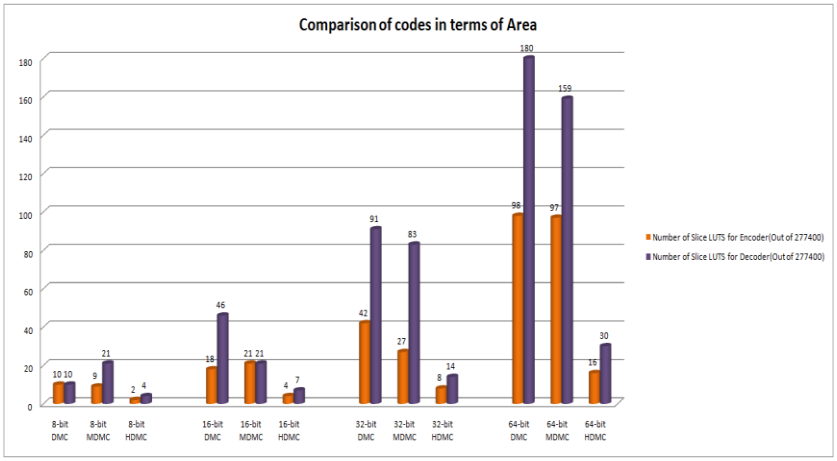

Figure5. Evaluation of Matrix Codes for Area

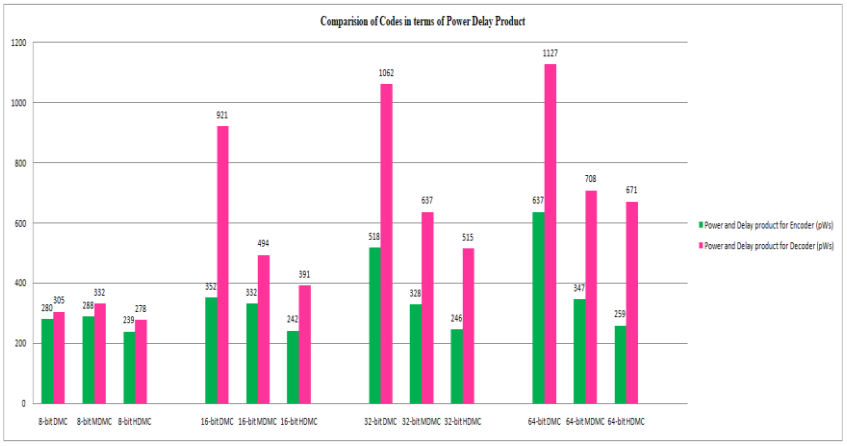

Figure6. Evaluation of Matrix Codes for Power Delay Product

The HDMC Code uses less area by at least 70.37% to 83.5% for encoder and 66.67% to 83.13% for decoder. Also the power delay product is minimized at least by 14.64 to 25.36% for encoder and 5.2% to 20.85%, as shown in figure 5 and figure 6. Hence HDMC Code proves to be efficient.

Table.1. Comparison of various codes with varying data lengths for various parameters

Parameters	DMC	MDMC	HDMC	DMC	MDMC	HDMC	DMC	MDMC	HDMC	DMC	MDMC	HDMC
# Data Bits, k	8	8	8	16	16	16	32	32	32	64	64	64
# Parity Bits, r	12	10	7	20	18	11	36	34	19	68	66	35
# Code Word, n=r+k	20	18	15	36	34	27	68	66	51	132	130	99
Bit Overhead, r/k in %	150	125	87.5	125	112.5	68.75	112.5	106.25	59.37	106.25	103.125	54.69
Code Rate, k/n in %	40	44.4	53.33	44.44	47.06	59.26	47.06	48.48	62.74	48.48	49.23	64.65
Code Efficiency, r/n in %	60	55.56	46.67	55.56	52.94	40.74	52.94	51.51	37.25	51.51	50.77	35.35

The table 1 compares different codes for parameters such as bit overhead, code rate and code efficiency. The HDMC code reduces the bit overhead by at least 5.5% to 46.96%, code rate is improved at least by 16.74% to 23.85% and the code efficiency is found to vary from 16.67% to 30.37%.

5. CONCLUSIONS

The errors occur in images during transmission, there is a possibility of wrong diagnosis while treatment. To overcome this problem, EDAC Codes are proposed to maintain effective transmission by using channel coding techniques like Matrix codes. This project mainly concentrates on detecting and correcting the changes in received images, so that it enables exact diagnosis of patients. The implemented codes were represented in verilog hardware description language and tested in Xilinx ISE 14.5 Tool for XC7Z020-1CLG484 FPGA. The HDMC code is efficient for area and power delay product. As compared to DMC and MDMC Codes, it reduces the bit overhead and improves code rate.

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