AN EFFECTIVE APPROACH TO REDUCE THE STANDARD CELL LOCAL UTILIZATION AND CONGESTION USING TCL

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ABSTRACT

TCL scripting language has become the de-facto standard for EDA tools. In physical design placement, CTS (clock tree synthesis) and routing playing major role. Due to improper placement and routing, utilization of standard cell area increases and congestion occurs. Because of congestion create some timing violations, shorts and DRC's. Logical levels, functionality, and latency values all have a significant effect on the timing. In this paper I am going to explain, how to maintain equal cell utilization across the design, how to control standard cell placement near macros / between the channels, how to control signal routing to reduce congestion.

KEYWORDS

Standard cell, Macros, Placement, Placement blockage, Signal routing, Routing guide, Congestion, ASIC.

1. INTRODUCTION

1.1 Placement

Digital electronic systems now absolutely dominate today's devices and designs. The method of identifying an appropriate position for predesigned cells on the chip is known as placement. The position of each standard cell on the die is determined by the tool. Placement can optimizing the design. The standard cell's location on the core is determined by the placement tool. The system's timing requirements, the length of interconnect and thus the connections between cells, power dissipation, and other factors all play a role.

The placement solution determines the length of the interconnect, and it is critical in deciding the system's efficiency as the geometries shrink. The placement variations are global placement, local placement, time-driven placement, congestion-driven placement and power-driven placement, ECO placement.

Coarse placement and legalisation are the two levels of placement.

1.1.1. Coarse placement

The placement tool calculates an estimated locations for predesigned cells during coarse placement based on some cost functions. There is a chance of standard cell overlapping if

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the cells are not aligned with placement grid. For initial timing and congestion analysis, coarse placement is fast and accurate.

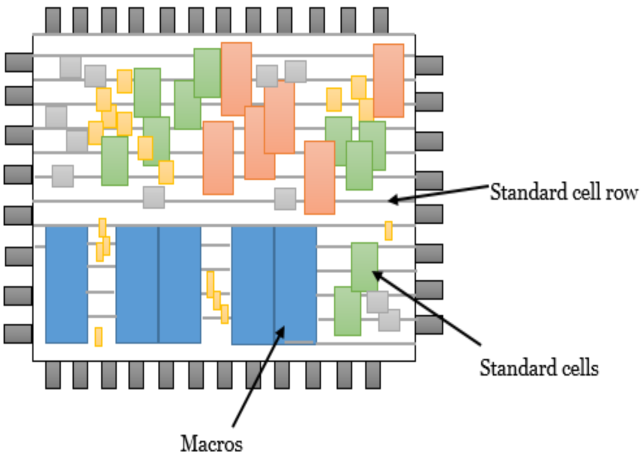

Figure 1: Coarse placement of cells

1.1.2. Legalization

The placement tool guides the cells to correct positions on the placement grid and removes overlaps between cells during legalisation. The lengths of the wire connections change as a result of these minor changes in cell location, there is a possibility for new timing violations. In certain cases, those violations can be resolved by resizing the buffer size like upsize or downsize.

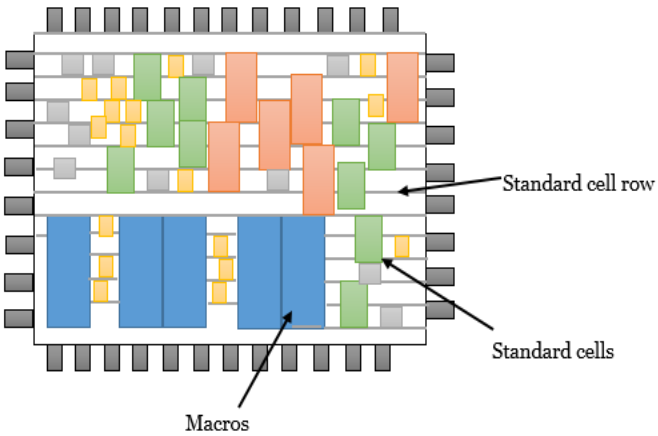

Figure 2: Legalization of standard cells

During placement optimization and legalization, the placement constraints providing guidance to minimise the congestion and timing violations.

1.2. Routing

Routing is the process of connecting the pins of a signal using metal wires while adhering to manufacturing design specifications. Cell placement, where the cells used in the design are located, must be completed before routing can be done on the design. It is necessary to connect the pins of the cells that belong to the same signal. Only logical relations exist between these pins at the time of placement. Routing is used to establish physical connections.

Routing creates physical connections to all data signals. Global routing, Detailed routing, and Track assignment are the three phases of routing.

1.2.1. Global Routing

The architecture is first divided into small boxes, each of which is referred to as a global routing cell (gcell), with each gcell containing a variety of horizontal and vertical routing resources. Global routing assigns nets to specified metal layers and global routing cells. We can analyse congestion by using global routing. Detouring is necessary if any of the gcells are congested.

1.2.2. Track Assignment

Tracks are allocated to each global route after global cell estimation. Each partition have tracks assigned to it in both vertical and horizontal directions. The metal used determines the routing direction; if m1 is horizontal, m2 is vertical. Global routes are replaced with metal layers at this phase, resulting in numerous drc and timing violations.

1.2.3. Detailed Routing

It means real routing metal connections. In this, physical drc's are also tested. Detail routing, unlike track assignment, doesn't work on the whole chip at the same time; as an alternative, it operates by rerouting within the boundaries of a small area known as a "sbox." sbox : for the detail approach, partition the block into smaller boxes.

1.2.4. Grid based and gridless routing

A routing grid is extrapolated on the routing region in grid based routing. The grid lines are used for routing. The distance between neighbouring grid lines is measured in wire pitch. Any model that does not use grid-based routing should be avoided. on the other hand, is referred to as a girdles routing model. This model is more difficult and time-consuming than grid-based routing, but it is ideal for wire sizing and perturbation. To put it another way, grid-based routing is lot less difficult to enforce.

2. BACKGROUND AND MOTIVATION

2.1. Placement

Placement can be done in four optimization phases.

1. Pre-placement optimization:

   The netlist before placement is optimised, HFNs are collapsed. It may also reduce the size of the cells.

2. In placement optimization:

Based on VR, reoptimizing the logic and also performs cell sizing, cell moving, cell bypassing, splitting of nets, gate duplication, buffer insertion, area recovery. The time-driven placement and congestion driven placement are performed through optimization.

3. Post Placement Optimization (PPO):

The PPO performs optimization of netlist with ideal clocks before CTS. It has the ability to fix setup, hold, max transition violations. It can optimise placement based on global routing. It re-synthesizes HFN.

4. PPO after CTS:

The PPO after CTS optimizes timing with propagated clock. It attempt to keep the clock skew.

2.1.1. Congestion

If the available routing tracks are less than the number of necessary routing resources, congestion occurs. We can see this situation in global routing. A congestion map will assist us in visualising the placement standard. The boundaries between global routing cells are highlighted with different colours to reflect different levels of overflow on the congestion map. The selected layers' overflow and underflow.

2.1.2.1 Congestion occurs due to following reasons

If the local utilization of standard cells is high, due to bad floorplan nothing but like without proper blockages in the chip area, due to the nets of the channels between the macros. Macros/standard cells may have used all of the metal layers within, resulting in less routing resources. Placing macros in the middle rather than the boundary, and using the IO optimization tool to buffer a large number of cells are placed in core area.

2.1.2.2. How to control the Congestion?

Congestion can be caused by a high cell density. The cell density can be set to up to 95% by default. Using the coordinate option, we can minimize cell density in congested areas.

set congestion options –max_util 0.5 –coordinate {x1 y1 x2 y2}

The maximum cell density is set to 50% , and the coordinates for the specific area are given. By
default tool tries to spread all standard cells equally throughout the core area. With this behavior, sometimes cells will sit too far from each other. It leads to more net lengths and ney delays and eventually ends with timing degradation.

set_app_options –name place.coarse.auto_density_control –value1

When we enable auto density, Tool will decides the max density considering timing and total utilization.

When we set the max density value by using Below setting, Tool allows cells upto the specified value in timing critical zones (allows local density upto the specified value to meet timing).

set_app_options –name place.coarse.max_density –value 0.7

When we set the congestion max util value by using Below setting, Tool limits the local density in congestion critical areas

set_app_options –name place.coarse.congestion_driven_max_util –value 0.65

With the Below settings, Tool tries to reduce congestion with the cost of run time.

set_app_options –name place.coarse.congestion_effort –value high
set_app_options–name lace.coarse.congestion_layer_aware -value true

By Using partial placement blockages, you can lower the local cell density.

create placement blockage–type partial blocked_percentage 50 boundary { {$llx $lly} {$urx $y end}} – name pb_user

It means that 50 % area is reserved for standard cell placement and the other 50 % is open for standard cell placement.

The keepout margin command can be used to apply cell padding.

c*reate keepout margin –type soft –outer {10 10 10 10} my_lib_macro*

Macro padding nothing but providing additional space for macro pins to maintain the proper connections between the standard cells and macro pins.

2.2. Routing Congestion

Whenever the number of available routing tracks is less than the number of necessary tracks, routing congestion occurs and with the Below setting, Tool tries to reduce congestion with the cost of run time.

set_app_options–name route.detail.drc_convergence_effort_level –value high

3. OUR APPROACH

3.1. Create_placement_blockage

Placement blockages are areas where leaf cells must prevent overlapping some part of the placement blockage during placement and legalisation. There are two types of placement blockages: hard and soft. The placements of cells in the blockage region is prevented by a hard blockage. The course placer is prevented from placing cells in the blockage area by a soft blockage, but soft blockage area can allows the cells while optimization and legalisation. If the design has both hard and soft placement blockages then first priority goes to hard blockage.

A keepout margin is a region around the edge of your design's fixed macros where no other cells can be located.Creating a single big partial blockage not help accurately, as most of the cells might place at one location as shown in below figure 3. For this, we developed a tcl script to splitting the big partial blockage into multiple small partial blockages.

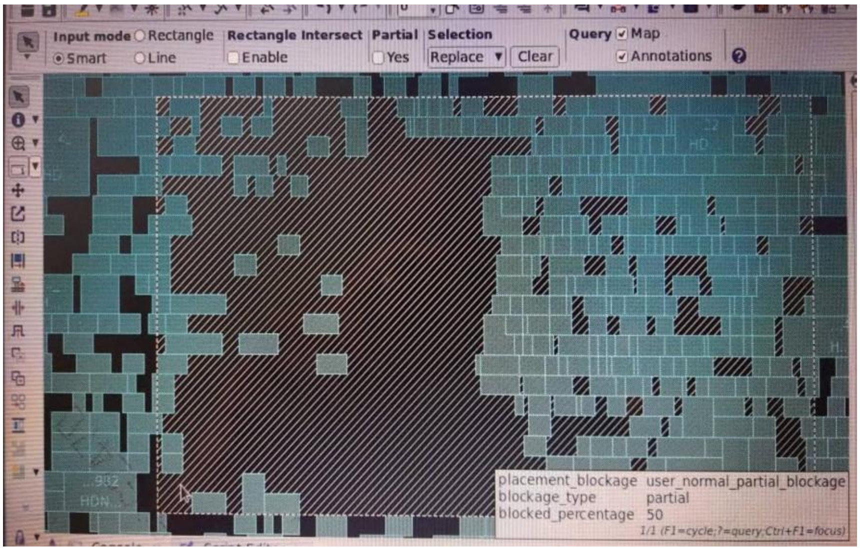

Figure 3. Default placement of standard cells

Creating partial blockages with given offset values, we can observe the big partial blockage at particular area is divided into small partial blockages and the standard cells are splitting equally as shown in the below figure 4.

create_placement_blockage-type partial locked_percentage $percentage -boundary \"{ {$llx $lly} {$urx $y_end}}\" -name pb_user

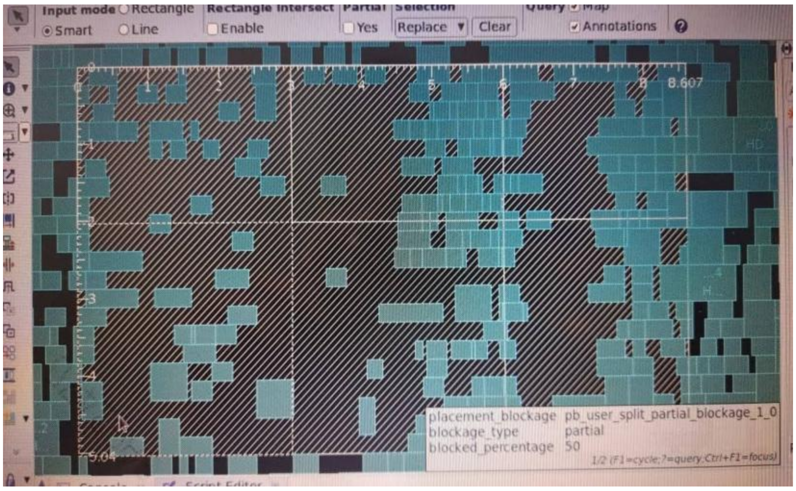

Figure 4. Placement with partial_blockages of size 3*3 μ²

Table 1. Default Placement Report of Asic Design

Area (microns)	Local utilization	Congestion	Pin density	DRC	Shorts
45 μ²	85%	3.2%	0.86	153	27

Table 2. Experimental Placement Report of Asic Design

Area (microns)	Local utilization	Congestion	Pin density	DRC	Shorts
Partial blockage with size (3*3 μ^2) for 45 μ^2	59%	0.5%	0.59	34	13

3.2. Create_routing_guide

Placement tool tries to utilize the top level metal layers for signal routing. It causes high utilization / congestion near to macros / IO ports and in a particular metal layer and area. Creating the one big routing guide not help accurately, as most of the routing tracks are placed at one location causes shorts and drc's as shown in below figure5. For this we develop a tcl script to split the one big routing guide into small partial routing guides.

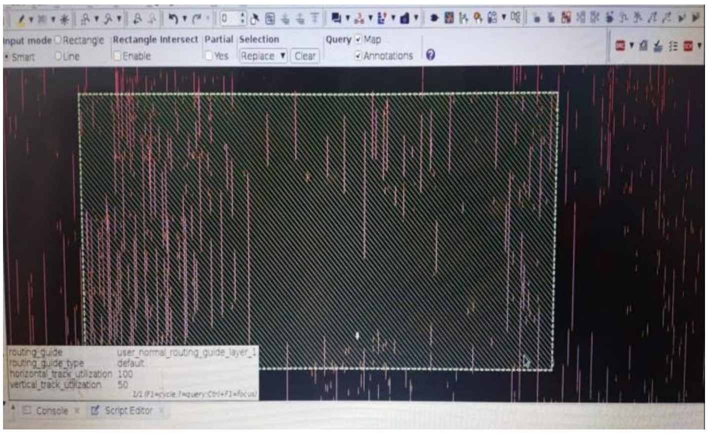

Figure 5. Default Routing_guide

Creating partial routing guides with given offset values, here we can observe the big partial routing guide at particular area of M5 layer (vertical) is divided into small partial routing guides and the utilization of signal routings is reduces for a particular area as shown in figure6. Due to this the design rule checks, shorts and congestion are decreases.

create_routing_guide -layers {M5 M6 M7 M8 M9 M10 M11}-preferred_direction_only horizontal_track_utilization $percentage -vertical_track_utilization $percentage -boundary \"{ {$llx $lly} {$urx $y_end}}\" -name rg_user

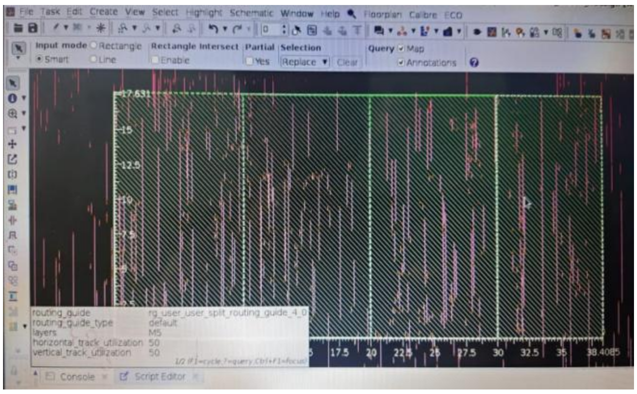

Figure 6. Routing_guide with partial_blockages of size 10*20 μ^2

Table 3. Default Routing Guide Report of Asic Design

Metal layer	Local utilization	Congestion	DRC	Shorts
M5 (Vertical)	79%	2.4%	96	23

Table 4. Experimental Routing Guide Report of Asic Design

Metal layer	Local utilization	Congestion	DRC	Shorts
M5	54%	0.4%	37	12

4. EXPERIMENTAL RESULTS

The following figure7 shows the default placement of standard cells in the ASIC design. We can observe the high local utilization, high pin density as well as high congestion.

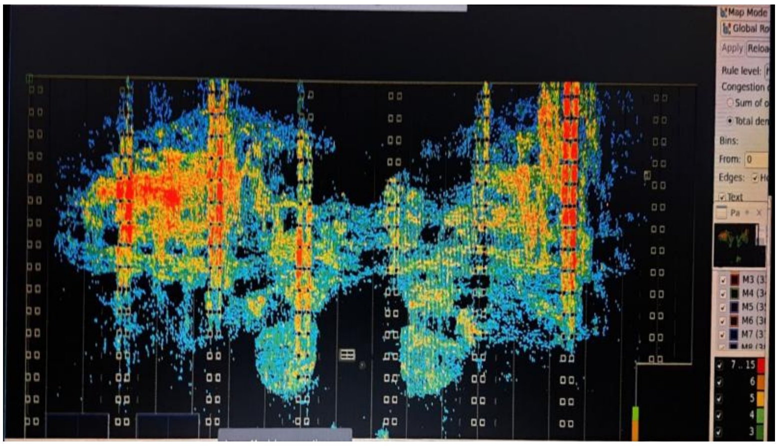

Figure 7. Initial or default congestion map

The following figure8 shows the placement of standard cells in the ASIC design with partial blockage of size 10*10micron sq for a particular location and we can observe the local utilization and congestion is decreases compared to default placement.

Figure 8. congestion map after creating partial blockages of size 10*10 μ^2

The following figure9 shows the placement of standard cells in the ASIC design with partial blockage of size 5*5micron sq for a particular location and we can observe the local utilization and congestion is decreases compared to placement with partial blockage size of 10*10 μ^2

Figure 9. congestion map after creating partial blockages of size 5*5 μ^2

The following fig11 shows the default routing guide of M1 vertical layer in the ASIC design. We can observe the high local utilization as well as high congestion.

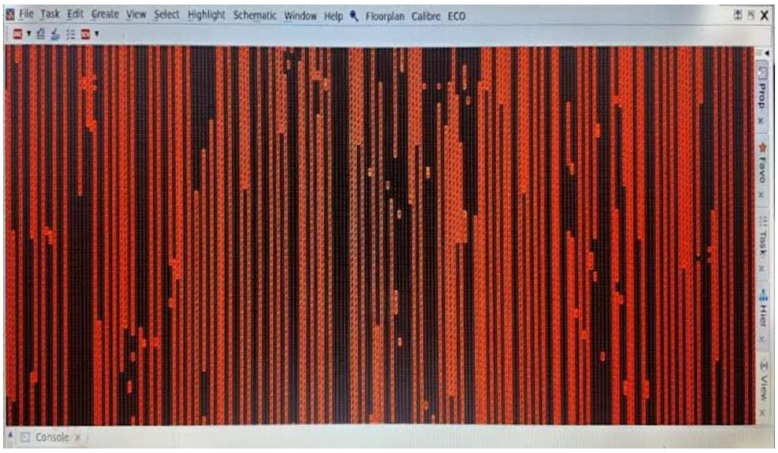

Figure 10. Default routing guide of M1 layer

The following figure11 shows the default routing guide of M5 vertical layer in the ASIC design. We can observe the high local utilization as well as high congestion.

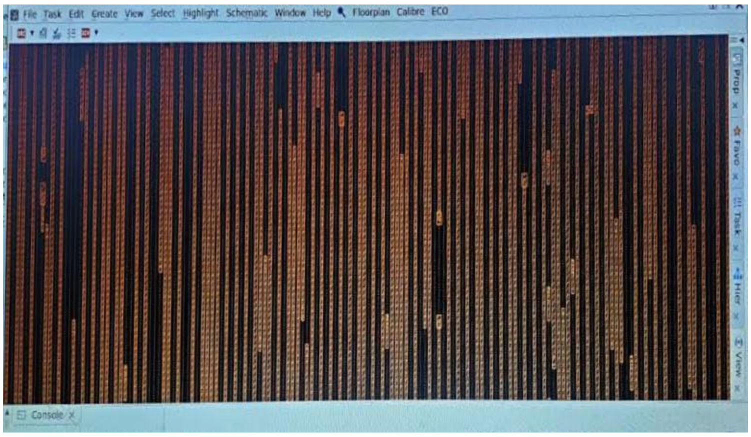

Figure 11. Default routing guide of M5 layer

The following figure12 shows the M1 vertical layer routing guide with partial routing guide of size 5*5 micron sq for a particular location and we can observe the utilization of routing tracks are decreases and congestion also decreases compared to default routing guide.

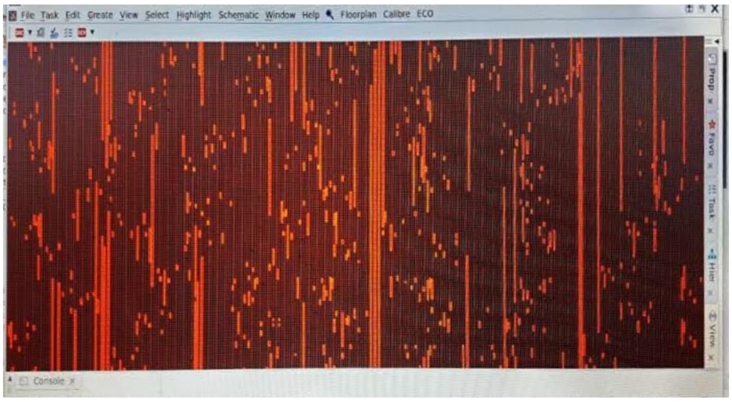

Figure 12. M1 routing guide after creating partial routing guides of size 5*5 μ^2

The following figure13 shows the M5 vertical layer routing guide with partial routing guide of size 5*5 micron sq for a particular location and we can observe the utilization of routing tracks are decreases and congestion also decreases compared to default routing guide.

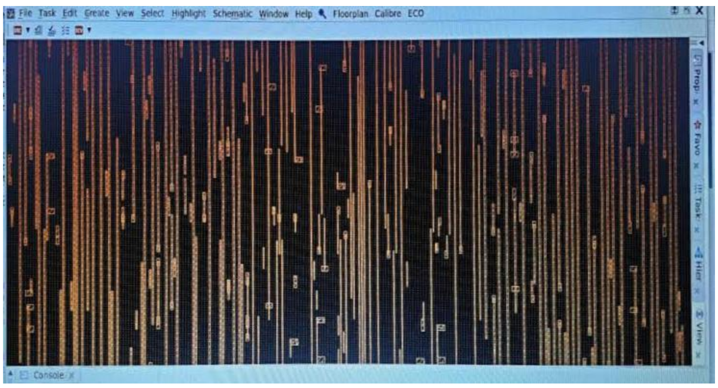

Figure 13. M5 routing guide after creating partial routing guides of size 5*5 μ^2

Table 5. Default Placement Report of Asic Design

Area (microns)	Local utilization	Congestion	Pin density	DRC	Shorts
9000 μ^2	60%	9.5%	0.64	7500	690

Table 6. Experimental Placement Report of Asic Design

Area (microns)	Local utilization	Congestion	Pin density	DRC	Shorts
Partial blockage with size (10*10 μ^2) for 9000 μ^2	53%	2.7%	0.55	2000	250
Partial blockage with size (5*5 μ^2) for 9000 μ^2	45%	0.7%	0.47	521	34

Table 7. Default Routing Guide Report of Asic Design

Metal layer	Local utilization	Congestion	DRC	Shorts
M1	81%	2.9%	1105	260
M5	85%	3.4%	1017	330

Table 8. Experimental Routing Guide Report of Asic Design

Metal layer	Local utilization	Congestion	DRC	Shorts
Partial blockage with (5*5 μ^2) for M1 layer	54%	0.4%	97	19
Partial blockage with (5*5 μ^2) for M5 layer	60%	0.5%	146	28

5. CONCLUSION

This paper presents a script based placement and routing methodology to minimize the standard cell local utilization and congestion by using P&R tool, ICC2, Synopsys. It is very flexible and can be used for almost any design since the entire design flow is based on scripts. In this work, using TCL script we divided a large partial blockage into small partial blockages for placement of standard cells in particular area and divide a large routing guide into small partial routing guides for signal routing in particular area and metal layer to maintain the equal cell utilization across the design, to control the standard cell placement near macros / between the channels, to control signal routing to reduce the congestion Although most EDA P&R tools support the TCL language, porting these scripts to other tools is very easy.

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