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DESIGN OF ALU USING 2T XOR GATE AND DECODER

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ABSTRACT

A design of Arithmetic and Logic Unit (ALU) with modified Gate Diffusion Input (m-GDI) as well as a design of ALU with 2T XOR GATE and DECODER are proposed in this paper. The use of modified Gate Diffusion Input in these techniques reduces the delay path, power consumption and area, as well as the number of transistors used. The power consumption is extremely low, resulting in a smaller footprint and a shorter delay path. The major components used in these techniques are the 2T XOR Gate in Digital VLSI Design based on Full Adder and Full Subtractor. Major, a fundamental novel The circuit for a 1-to-8 decoder was planned for different logic families before being implemented in an 8-bit Arithmetic and Logic Unit. EDA TANNER and Technique 180 nanometer Technology File are used to model the effects.

KEYWORDS

Arithmetic and Logic Unit(ALU) , VLSI Design, 2T XOR, DSCH 3.5, Modified Gate Diffusion Input (GDI)Tanner EDA and Technology File 180nm, and Verilog.

1. INTRODUCTION

The Arithmetic Logic Unit's main component is the Central Processing Unit (CPU). Arithmetic operations such as Addition, Subtraction, Multiplication, and Division are included in the CPU[1]. AND gate, OR gate, NAND gate, XOR gate, multiplexer. All of these operations are examples of logical operations. ALU operations necessitate a much larger number of capable computers, as well as application-specific circuits and VLSI chips. The results can necessitate sequential power requirements and power requirements across the entire processor.

The main function of designing larger are Low-power implementation and compact implementation Dissipation and these circuits are difficult to understand and they have no exception in ALU. Over the last few decades a lot of work has been taken to do in conventional CMOS based circuit and more impact power efficient [2-4]. Various techniques, such as Transmission Logic Gate, Domino Logic, Pass Transistor Logic, Double Pass Transistor Logic and others have been implemented in order to improve the performance of CMOS-based circuits [5-7].

The Gate Diffusion Input (GDI) technique is a novel approach for drastically reducing power requirements [8].Furthermore, GDI reduces the number of transistors, resulting in a smaller chip size, giving the designs an advantage over traditional methods [9].On the basis of GDI techniques, there are two types of transistors: PMOS and NMOS. Each of these has four subtypes: N.D.P and G [9]. G,N,P serve as inputs. However, GDI techniques have a big issue with gate diffusion input. [10] since NMOS generates logic 1 and PMOS generates logic 0. The existing GDI Technique is the major disadvantage. The use of modified GDI techniques results in a high efficient on CMOS

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and PTL.It can be used with an XOR gate and only two transistors using the m-GDI technique [12-14]. We may use two transistors in an XOR in these, which are based on various designs and come in a variety of forms. In a CMOS complete adder, there are 28 transistors used. It can be implemented with just 8 transistors using a 2T XOR complete adder [12].Furthermore, This paper employs a novel 1-to-8 decoder design that employs the GDI technique to allow only the desired ALU module to be selected via two select lines.

The following segments were introduced in the modified Gate Diffusion Input are:

• Arithmetic Unit: This unit is responsible for performing simple arithmetic operations such as addition and subtraction.
• Logical Unit: This component performs logical operations like OR, AND, XOR, NOT, and NAND gates are discussed in this article.
• To pick the desired input line, a buffer unit was used.

2. GATE DIFFUSION INPUT AND MODIFIED GATE DIFFUSION INPUT

In GDI, the key cell is CMOS, which can be used with an inverter circuit . It is capable of completing the mission in a more efficient manner. The circuit's various inputs are G, N, and P. G is the NMOS and PMOS common gate. The NMOS source terminal is N, and the PMOS source terminal is P. All of these are input terminals. D [9], a typical drain, is where the output is collected. Fig 1 depicts the diagram based on the number of functions; it can perform a number of primitive cells using the GDI approach. In tabular column, the inputs and outputs can be displayed. It can do a huge number of operations and contains a few GDI primitive cell flaws. It could be predicated on the number of primitive cells being increased or decreased.

The challenge of fabricating using existing CMOS technologies is the most important problem [15]. As previously stated, there's also the question of swing degeneration. The m-GDI cell, a modified version of the GDI cell with the PMOS and NMOS bulk terminals attached to VDD and field, respectively, has been designed to address these issues. Some of the logical circuits in the ALU were constructed using the GDI methodology; Others were created using the m-GDI methodology. Fig2 depicts the diagram of a simple primitive m-GDI cell.

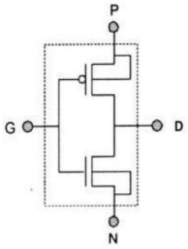

Fig 1: Primitive cell of Basic GDI

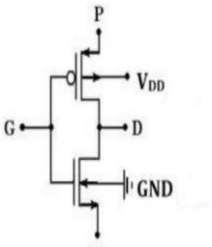

Fig 2: Primitive cell basic of m-DI

Table 1: Different types of Primitive cells and their functionalities

P	N	G	Output	Function
1	0	A	A’	NOT
A	B’	B	A’B+AB’	XOR
A	B	B’	AB+A’B’	XNOR
B	1	A	A+B	OR
A	B	S	AS’+BS’	2:1 MUX
B	0	A	A’B	Function 1
0	B	A	AB	AND
1	B	A	A’+B	Function 2

3. 2TXOR

With the use of two transistors, we can transform the XOR Gate utilizing the m-GDI approach, as illustrated in Fig 3. Both XOR gates are proposed to the ALU using the GDI technique.

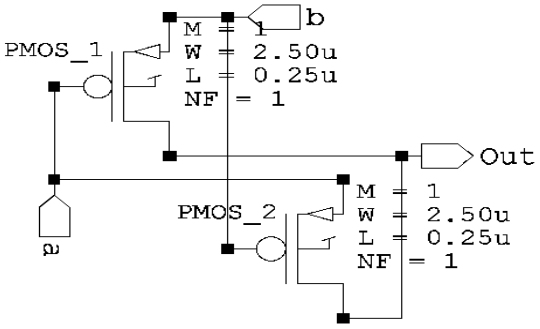

Fig. 3: m-GDI is used in the design of a 2T XOR.

The proposed ALU contains only 2T XOR gates. As a result, the total number of transistors in the circuit, as well as the total power consumption, has decreased significantly. One input (A) is connected to the pMOS source and gate terminals, while the other (B) is connected to both the pMOS general gate input terminal and the nMOS source terminal. The transistors' output terminal is the typical drain terminal.The resulting 2T XOR has only one transistor delay. The output logic level does, however, come with the disclaimer that it can become skewed at times. In comparison, In , Dan Wang et al. demonstrated that the correct logic level at output can be guaranteed at all times by varying the W/L ratio.Fig 1 shows the full adder [12] and full subtractor built with this 2T XOR 4a.

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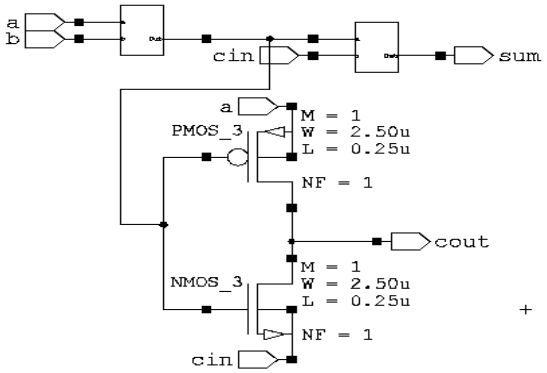

Fig4: 8-Transistor Full Adder Circuit Using 2T XOR Gate

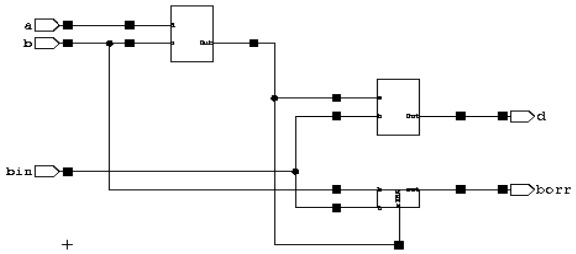

Fig 5: 2-Transistor Full Subtractor Circuit Using 2T XOR Gate

4. KEY COMPONENTS OF PROPOSED ALU

GDI has been used to implement AND, OR, NAND, and NOT gates, as well as MUX, comparator, and buffer circuits [8,17]. These circuit diagrams are shown below, from Fig. 6 to Fig. 11. When a buffer circuit is used, it is easier to choose the desired input when it is needed. When operating with other large circuits, the buffer circuit preserves the output while also adding a slight delay. Fig 11 illustrates the buffer circuit.

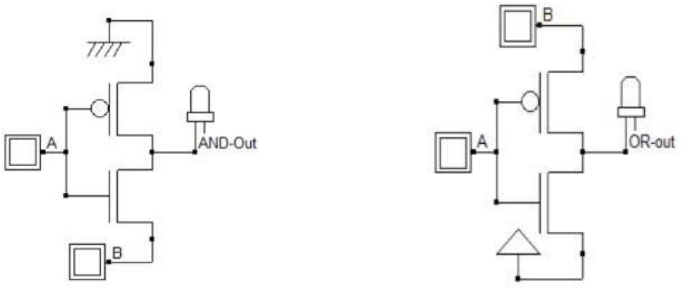

Fig 6: GDI Technique Using 2 Transistors AND Gate & 2 Transistor OR Gate

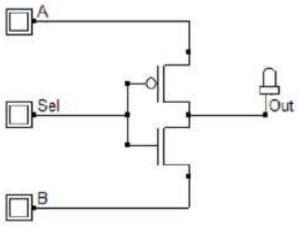

Fig7:2transistors Circuit Using GDI

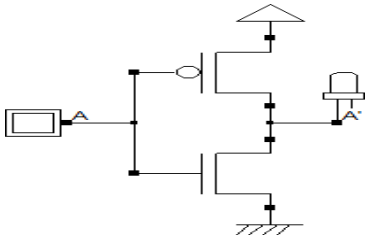

Fig 8: 2 Transistors Circuit Not Using GDI

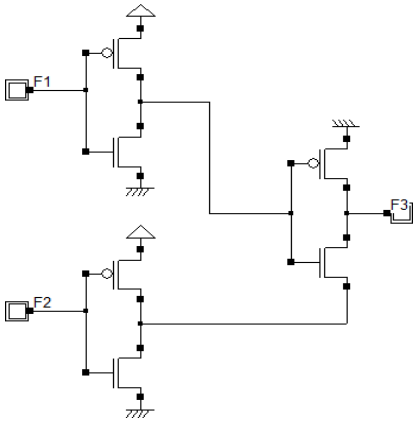

Fig 9: GDI Technique Using Comparator

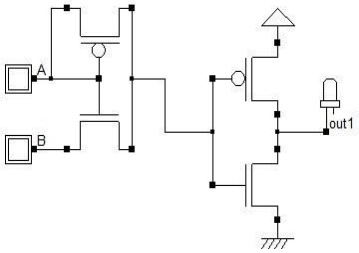

Fig 10: GDI Technique Using NAND Gate

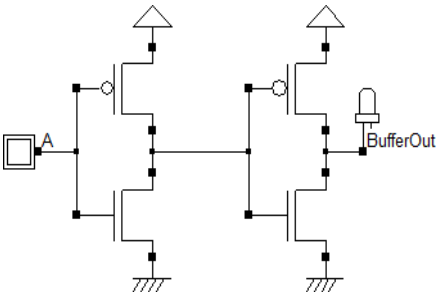

Fig 11 GDI Technique Using Buffer

So far, we've covered all of the ALU's core blocks; now it's just as important to have a framework that allows us to select any logical or arithmetic module. To do so, select and allow the desired circuitry using a 3-to-8 decoder and sixteen sleep transistors (2 per module). The decoder is one of a kind since it uses GDI Primitive cells

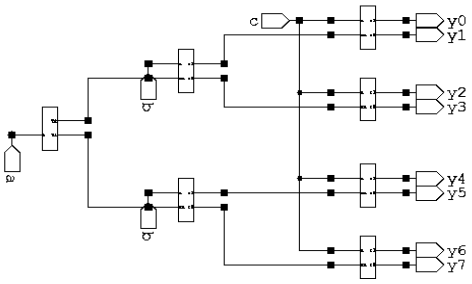

Fig 12: Decoder 1-To-8 Basic Circuit Diagram

Below is the inside circuit diagram for the 14 identical blocks that were utilized 14 times. It's just a simple three-to-eight decoder written in GDI.

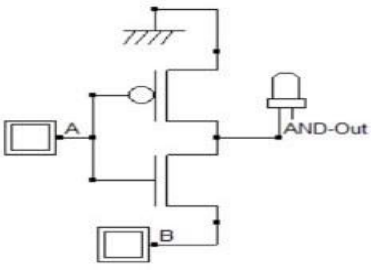

Fig 13: GDI Technique Using1:2 Mux

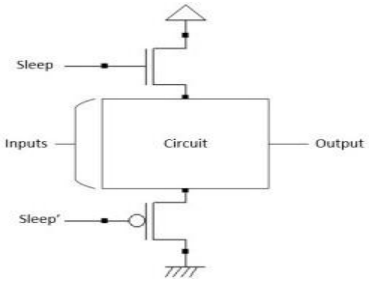

Fig 14: Simple Diagram Of Sleep Transistor

Sleep transistors are used to keep circuits inactive. When the signal Sleep=0 is set to normal standby mode,The sleep transistors turn on and the circuit is activated. For our convenience, we've inverted it so that when Sleep=1, the sleep transistors will be activated. A sleep transistor circuit diagram is shown below.

When all of these bits and pieces were combined, the ALU circuit shown in Fig. 15 resulted.
For demonstration purposes, bricks were used to replace the internal circuitry of critical modulesDetailed circuit schematics for all of the circuits, however, are provided above.

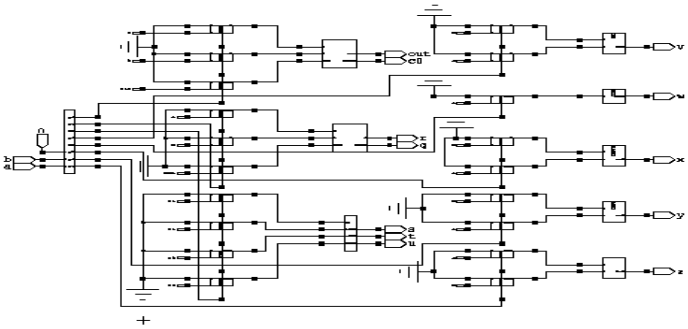

Fig 15 : Full Proposed Diagram With Aluminum Use Of A 2T XOR Gate In A Circuit

5. SIMULATION AND RESULT

Starting with transistor level design, the simulations were carried out using W-EDIT and S-EDIT, and then verified using Tanner EDA setting. All of the individual components that were realized using m-GDI, GDI, and CMOS logic were simulated and the results were presented.

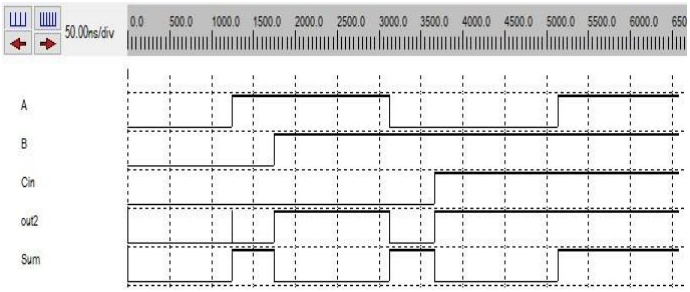

Fig 16: Simulation Wave Forms For 8transisitor Full Adder

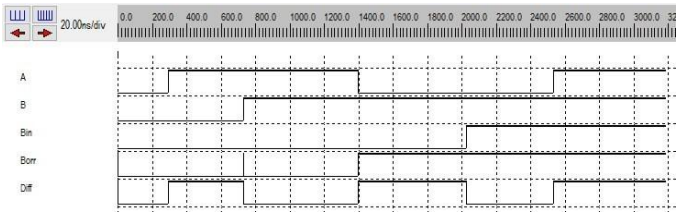

Fig 17:Simulation Waveforms For 8transistor Full Subtractor

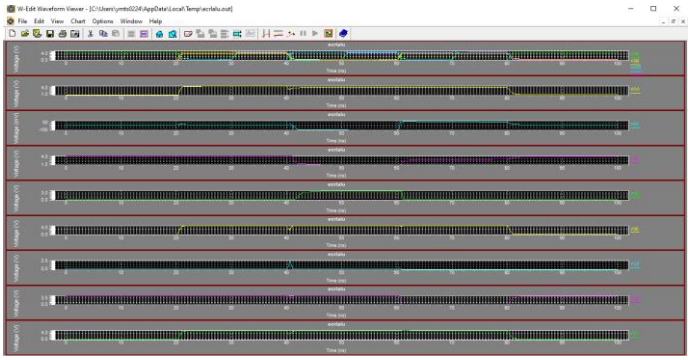

Fig. 18: Simulation Waveform Of 1-To 8 Decoder

The ALU is Tanner EDA's basic simulation waveforms have been defined as follows.

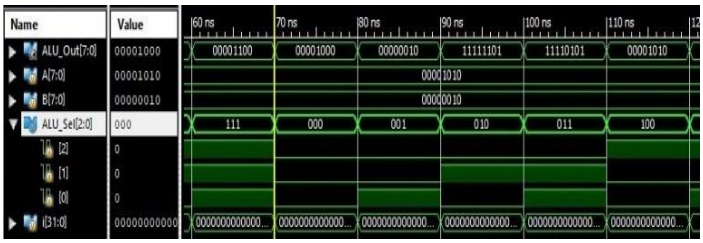

Fig. 19 : Simulation Wave forms of ALU–I

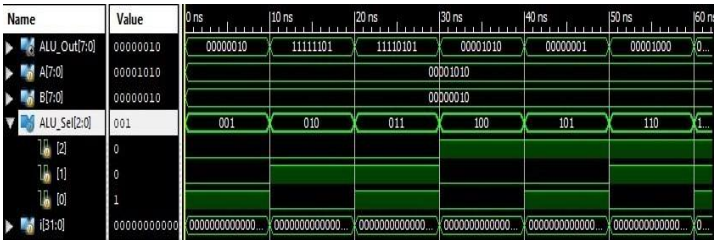

Fig. 20: Simulation Wave forms of ALU–II

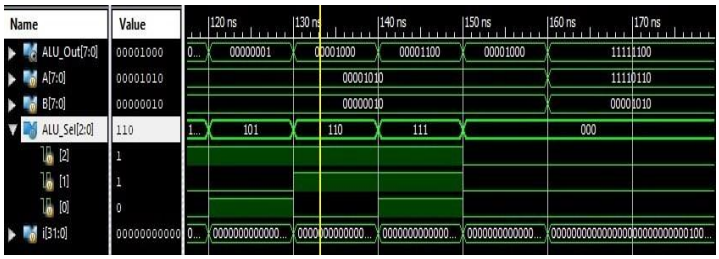

Fig. 21: Simulation Wave Form of ALU III

6. CONCLUSION

Table 2 compares our proposed model to the two other models mentioned in [8] and [11].

Table 2. Different Comparison of ALU

Design of ALUs	Power (nW)	Delay [(Critical path)-(ns)]	Count of Transistors
8 Bit ALU [8]	5.04	1.1	125
Proposed System	3.5	0.7	120

As shown in the table, Not only does the proposed ALU have the fewest transistors, but it also outperforms the others in terms of power and critical path latency.. As can be seen, the proposed model outperforms conventional models. Tanner is used to simulate the design at 180nm technology. EDA simulations show that the proposed ALU takes up less space and has a shorter power cycle.

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