TEMPERATURE SENSOR WITH BUFFER-CHAIN BASED TIME-TO-DIGITAL CONVERTER FOR ULTRA-LOW VOLTAGE OPERATION

Kaito NAGAI[1] and Kimiyoshi USAMI[2]

[1] Graduate School of Engineering and Science, Shibaura Institute of Technology, Japan
[2] Department of Computer Science and Engineering, Shibaura Institute of Technology
SIT Research labs. International Research Center for Green Electronics

ABSTRACT

This paper proposes a Time-to-Digital Converter (TDC) based temperature sensor that aims to operate with an ultra-low voltage electromotive force for IoT applications with energy harvesting. Sub-threshold circuit design was exploited for the operation at ultra-low supply voltage. The proposed circuit uses the characteristics of leakage current for temperature measurement. The virtual ground node in the proposed sensor is charged up by leakage current and the charging time changes with the temperature. To measure the temperature-dependent charging time, we used a buffer-chain based TDC to achieve ultra-low voltage operation. Simulation results demonstrated that the minimum supply voltage for the proposed circuit is 0.15V. The power consumption is 407nW and sensing time is 180ns at 25℃. The measurable temperature range is from -40℃ to 85℃. The proposed circuit was designed with Renesas SOTB 65nm process. Simulation evaluation was conducted using HSPICE.

KEYWORDS

Temperature sensor, ultra-low voltage, Time-to-Digital Converter, Sub-threshold

1. INTRODUCTION

With the rapid spread of Internet-of-Things (IoT) in recent years, IoT devices such as sensor nodes have been developing. Since IoT devices are battery-powered, they must operate for long periods of time with limited power consumption, so low-power technologies are important. In addition to providing power to operate a huge amount of IoT devices, energy harvesting is a way to make batteries life keep longer [1]. When using energy harvesting, such as thermoelectric power generation, the electromotive force may be ultra-low voltage, requiring circuit designs that operate at ultra-low voltage [2]. A temperature sensor is an important component used in IoT sensor nodes. Various smart temperature sensors using CMOS technology have been studied.

The Analog-to-Digital (ADC) type temperature sensor measures temperature by converting the difference in voltage that varies with temperature using an ADC. The previous work [3] measured temperature by connecting a temperature dependent resistor in series with a capacitor Digital-to-Analog Converter and using an ADC to sample the RC time constant and convert it to digital outputs. The circuits of this temperature sensor operate at supply voltage of 0.6V. The ADC type temperature sensors have weaknesses such as sensing errors and increased power consumption [4]. For this reason, ADC are frequently avoided. It is also difficult to operate at ultra-low voltages.

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The TDC type temperature sensor measures temperature using the delay time difference between signals that varies with temperature. TDC [5] is a circuit that measures the time difference between two signals START and STOP and consists of multiple buffers and latches. Initially, the signal to start measurement is input to the Delay line to which the buffers are connected in sequence as a START. When the START signal is input to the buffer, the output of each buffer raises the output of each latch. At this time, as shown in the timing chart in Fig. 1, the timing at which the output of the latch rises differs due to the buffer delay. The signal to be measured is input to the EN signal of the latch as STOP to fix the output of the latch. The outputs of all latches allow the time difference between two signals to be expressed in terms of the number of buffer stages.

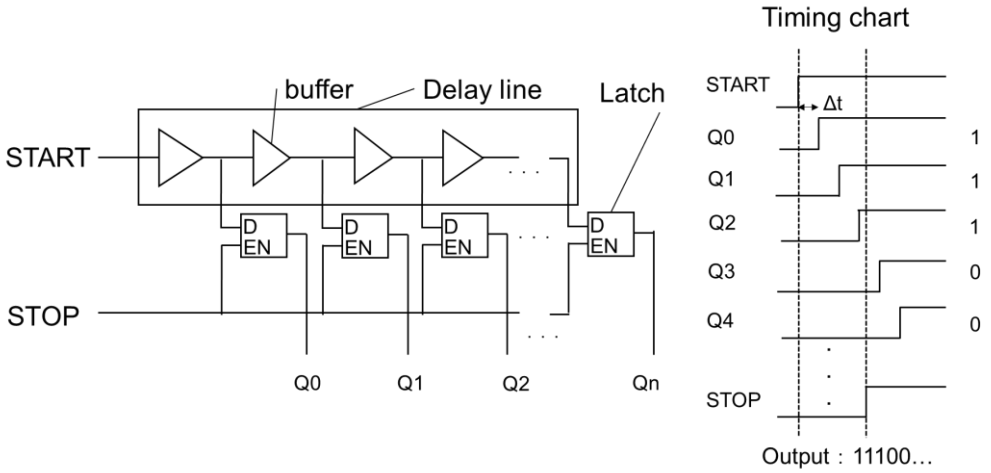

Figure 1. Structure of Time-to-Digital Converter circuit and example of timing chart

The paper [6] on temperature sensors using TDC has utilized Pulse-Width Modulation (PWM) signals whose duty cycle is proportional to absolute temperature. Temperature is measured by measuring the duty cycle of the PWM signal generated by the BJT at TDC and converting it to temperature. This temperature sensor is reported to operate at a supply voltage of 1.4V.

The paper [7] uses an oscillator that generates a frequency that varies proportionally to the temperature. First in the principle of the circuit of this work, a proportional-to-absolute-temperature (PTAT) current source is realized by a register whose current increases linearly with temperature. The PTAT current is mirrored using a bit-weighted current mirror (BWCM) to starve a current-controlled oscillator (CCO) to generate frequencies proportional to the temperature. The generated frequency is then digitally coded and converted to the temperature. This temperature sensor operates at 0.2V.

An on-chip leakage monitor type temperature sensor using sub-threshold leakage current has been proposed as a temperature sensor for ultra-low voltage [8,9]. Sub-threshold circuits use supply voltages below the threshold voltage to achieve ultra-low operating voltage and low power consumption. An on-chip leakage monitor type temperature sensor consists of a leakage current generation circuit, a Voltage comparator, and a Monitor controller including a counter as shown in Fig. 2. Fig. 3 shows the structure of Voltage comparator. In this temperature sensor, the measurement is initiated by turning off the Power Switch (PS) of leakage current generation circuit. This gradually charges the virtual ground line (VGND) with leakage current through the pMOS transistors. The VGND line is input to the Voltage comparator as a signal, and when the VGND voltage reaches the reference voltage, the output to the Monitor controller changes to 1 as

the Comparison result. Monitor controller counts the clock cycles using the counter until the Comparison result is given. Since leakage current is temperature dependent, the Monitor result will vary with ambient temperature. In other words, as the temperature gets lower, the leakage current decreases, so the charging time of VGND becomes longer and the counter value becomes higher.

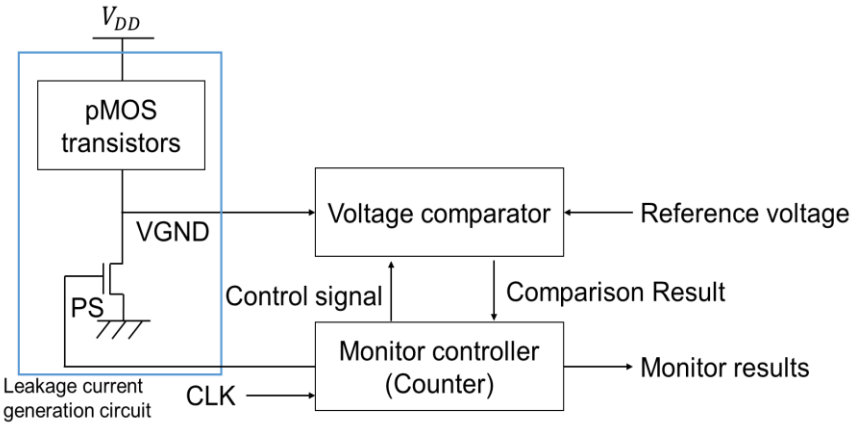

Figure 2. Structure of on-chip leakage monitor type temperature sensor

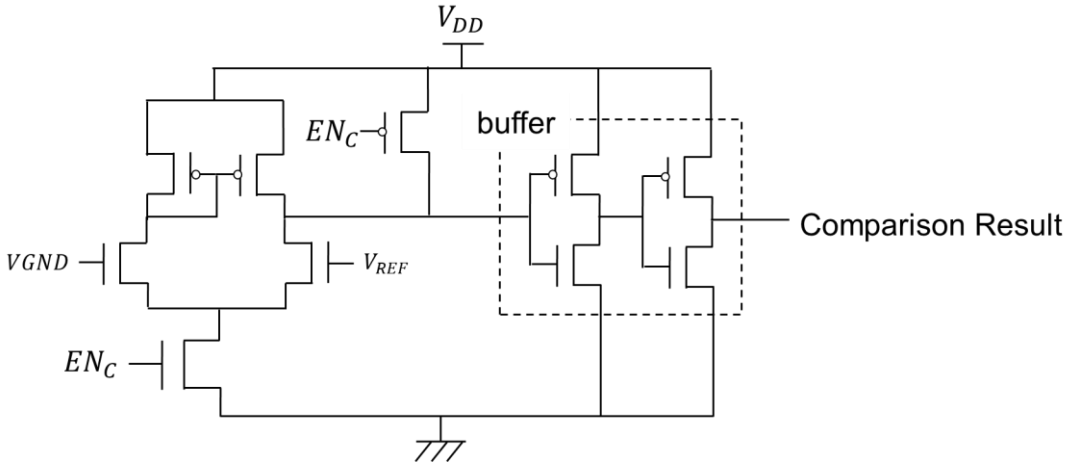

Figure 3. Structure of Voltage comparator

Previous temperature sensor has been confirmed to operate at the supply voltage of 0.25V, but at lower voltages, the counter circuit in the Monitor controller did not operate. Furthermore, it was reported that the Monitor controller accounts for most of the power consumption [9].

In this paper, we propose a novel circuit that can operate at the voltages lower than 0.2V and achieve low power consumption by using alternative circuits for the counter.

This paper is organized as follows. Section 2 presents the architecture of the proposed temperature sensor circuit, and Section 3 shows the experimental results. Conclusion is given in Section 4.

2. PROPOSED APPROACH

2.1. Structure of proposed temperature sensor

The proposed circuit consists of a leakage current generation circuit and TDC, as shown in Fig.4. The VGND voltage was measured by the Voltage comparator but is configured to be input to the inverter. The Voltage comparator is activated when the PS is turned off, and if the temperature is low and the charging time is longer, the activation state is prolonged and power consumption increases. In addition, an externally input reference voltage is no longer required, and the circuit area can be reduced. TDC consists of 64-stage buffers and latches. The conventional TDC uses DFF, but the new configuration uses latches. The use of a latch reduces the clock input and allows the circuit to be designed for ultra-low voltages, as shown in Section 2.2.

In the initial state, the START signal is set to the logic value 0. Therefore, the outputs of the buffers in the Delay line are also logic value 0. On the other hand, since the PS signal is 1, the VGND voltage is 0V. This means that the STOP signal is initially set to 1. Since the latches pass the input data through to the outputs, the outputs Q0 to Q63 of the latch become all 0. When the START signal is set to a logic value of 1, the outputs of the buffers in the Delay line and latches change to 1 in turn. At the same time, in the leakage current generation circuit, the VGND voltage is gradually charged. The output of the inverter becomes logic 0 when the VGND voltage goes up to the logic threshold voltage of the inverter the STOP signal becomes 0 and the outputs Q0 to Q63 are fixed.

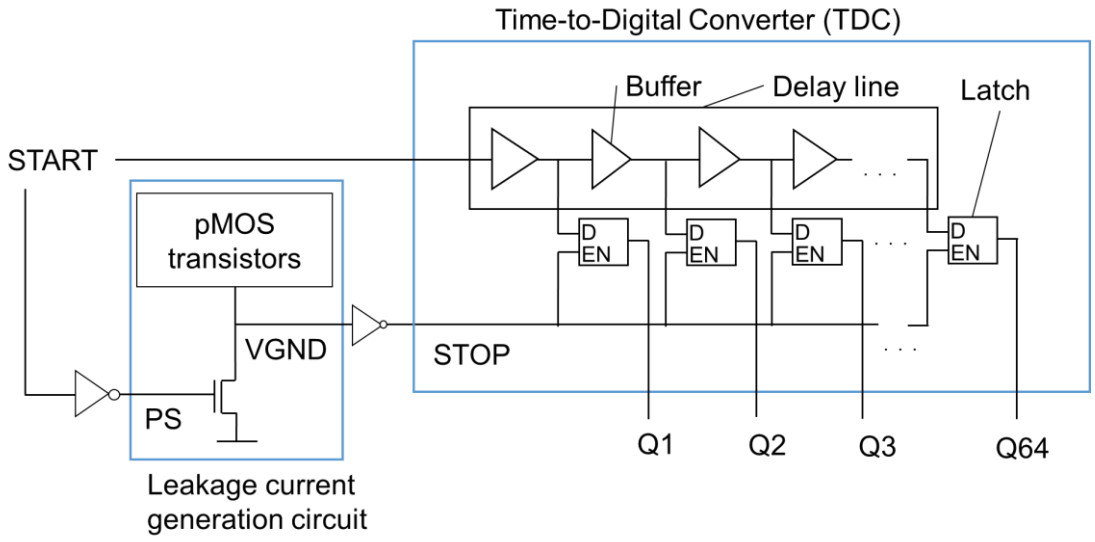

Figure 4. Structure of the proposed circuit

Due to the temperature dependence of the leakage current, the time to charge up the VGND line varies with temperature, and the timing at which the output of latch is fixed varies accordingly. Since the timing at which the output of a latch becomes 1 varies depending on the buffer delay, the number of latch stages whose output becomes 1 changes. Temperature can be measured by converting the number of latch stages whose output is 1 to the temperature. For example, when the temperature is lower, the leakage current decreases, so the charging time of VGND line becomes longer. As a result, the timing when the output of the latch is fixed becomes slower, and the number of latch stages whose output is 1 increases. Conversely, the leakage current increases at high temperatures, which shortens the charging time of the VGND line and reduces the number

of latch stages with an output of 1. Timing charts for lower and higher temperatures are depicted in Fig. 5.

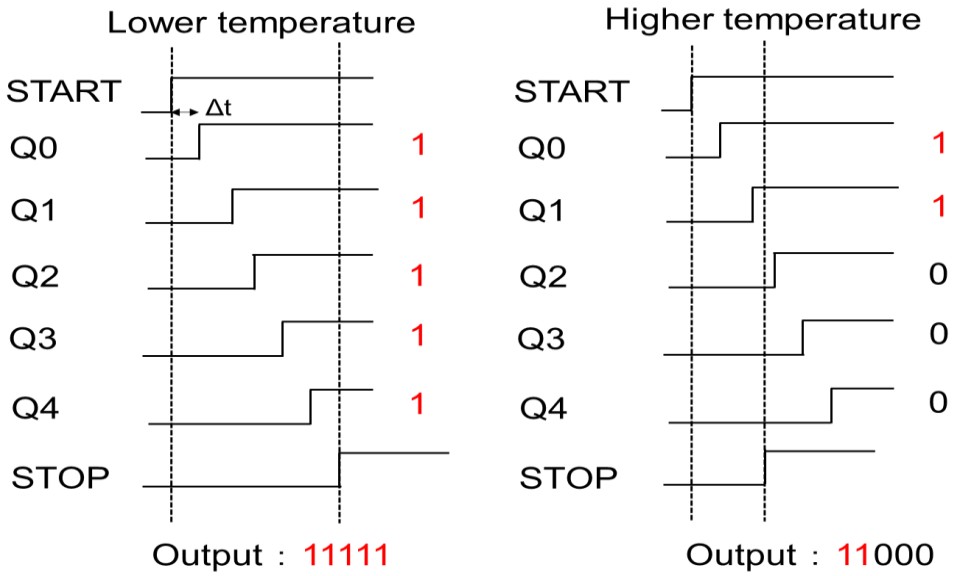

Figure 5. Example of timing chart depending on the temperature

2.2. Latch circuit with Clocked Inverter for ultra-low voltage

As a latch circuit used in TDC for ultra-low voltage, we propose to employ a latch circuit using a clocked inverter (CINV latch) [10] shown in Fig.6. We first tried a latch circuit using a transmission gate (TG latch) shown in Fig.7 which is employed in a typical flip-flop circuit [11]. This is because a TG latch has less transistors than the CINV latch.

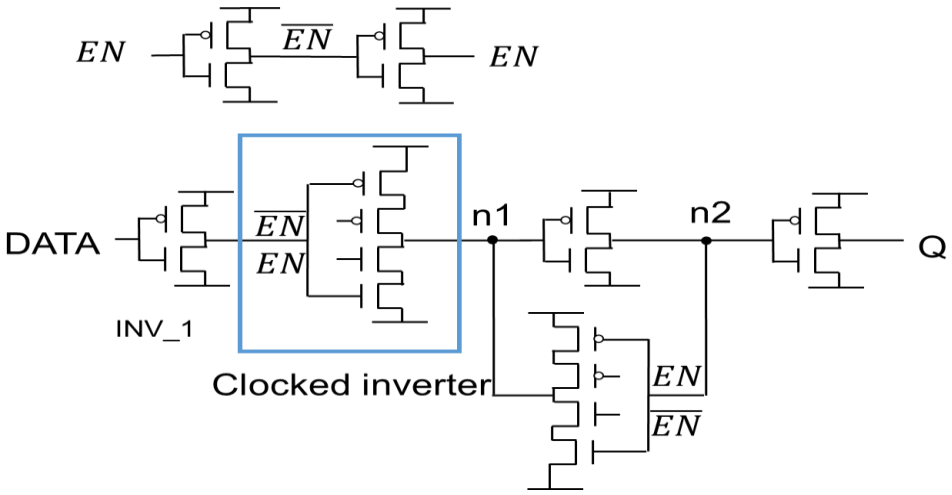

Figure 6. Latch circuit with clocked inverter

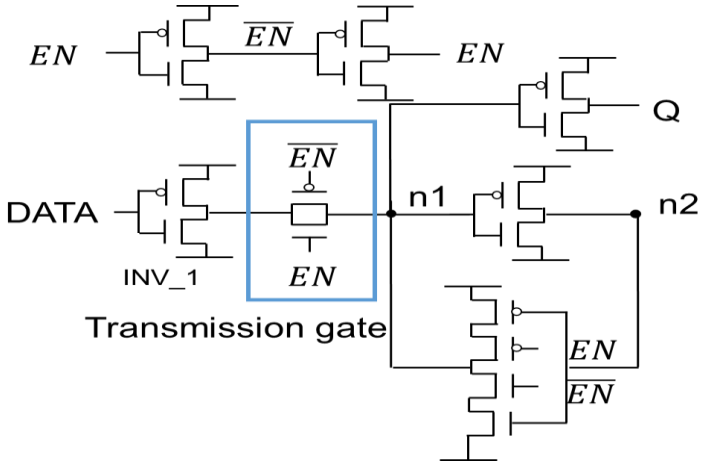

Figure 7. Latch circuit with transmission gate

As a result of simulations for both circuits, it turned out that the TG latch cannot hold its value even when the EN signal is set to 0 under high temperature conditions, resulting in unstable output. Simulation results of the TG latch and CINV latch at high temperature conditions are shown in Fig.8 and Fig.9, respectively. For Fig.8, node n1, node n2, and output Q must remain in the same state while the EN signal is logic 0 from 30ns to 60ns. However, the voltage of node the n1 drops and the voltage of the n2 rises accordingly, resulting in being unable to hold the output Q. We think this is due to a leakage current flowing through the transmission gate in off-state and the nMOS transistor of the inverter INV1 to the ground in front of the transmission gate despite the EN signal being logic 0. The voltage drop at the node n1 is amplified by the inverter-CINV loop, resulting in erroneously flipping over the output value at Q. On the other hand, as shown in Fig. 9, the CINV latch is able to maintain the state of node the n1 and the n2 and output Q while the EN signal is at logic 0. From the above simulation results, we use the CINV latch in the proposed circuit.

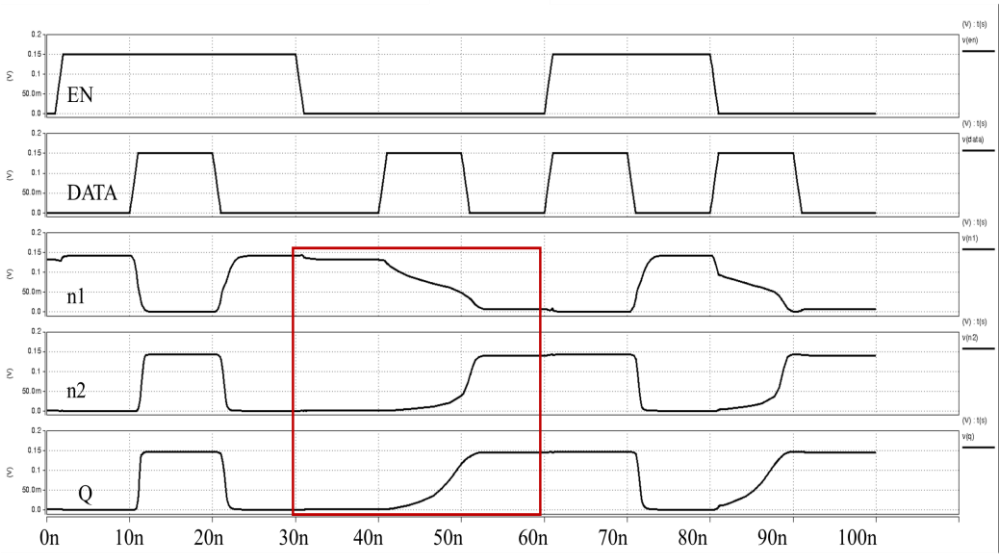

Figure 8. Simulation results of TG latch under high temperature conditions.

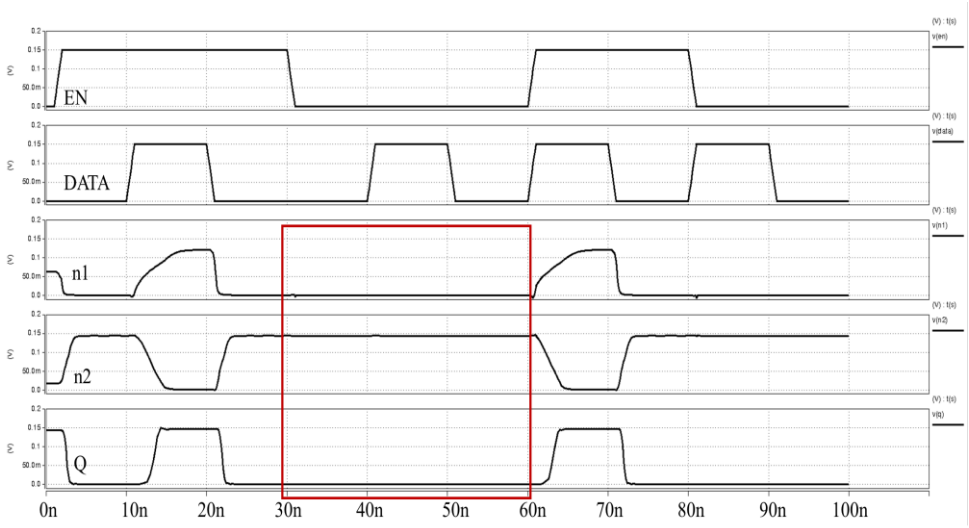

Figure 9. Simulation results of CINV latch under high temperature conditions.

3. EXPERIMENTAL RESULTS

We designed the proposed temperature sensor in a Renesas 65nm process. Similarly, the previous temperature sensor in Fig.2 was designed in the same process technology and evaluated by HSPICE simulation. Firstly, the operable voltage of the previous temperature sensor was simulated by lowering the operating voltage by 0.01V from 0.25V, and the minimum supply voltage was measured. As a result, it turned out that the minimum operating voltage VDD_MIN of the previous temperature sensor was 0.2V. Simulation results for the proposed circuit showed that the proposed circuit with 64 buffers and latch stages successfully operates at the supply voltage of 0.15V within the environmental temperature range from -40°C to 85°C. Fig.10 shows the number of latch stages whose output is 1 at each temperature. As mentioned above, the number of latch stages whose output is 1 increases at lower temperatures and reduces at higher temperature. Fig.11 shows the counter value of the previous temperature sensor. Similarly, the counter value is smaller when the temperature is high and larger when the temperature is low. Based on these results, the minimum supply voltage was set to 0.15V for the proposed temperature sensor, and 0.20V for the previous temperature sensor. Simulations were conducted for power consumption, sensing time, energy consumption, and resolution.

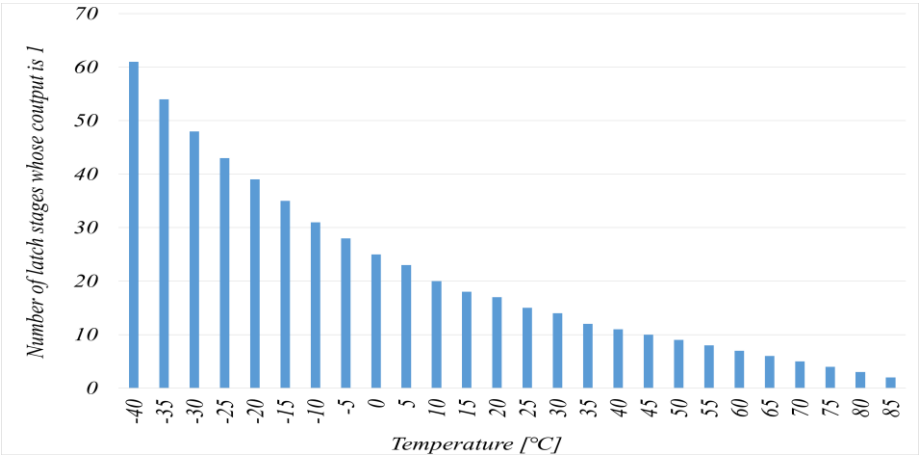

Figure 10. Output results of the proposed circuit at 0.15V

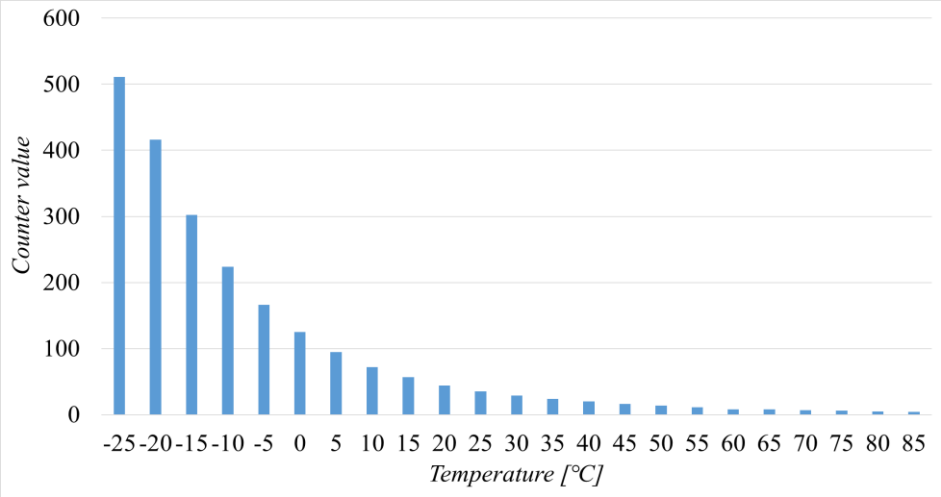

Figure 11. The counter value of the previous temperature sensor

3.1. The simulation results for the operation of the proposed temperature sensor

Fig.12 and Fig.13 show the simulated waveforms for the operation of the proposed temperature sensor circuit at 20°C and 25°C, respectively. When the START signal rises from logic 0 to logic 1, PS is turned off and the VGND voltage starts to rise. In the meantime, the outputs of the latches become 1 from left to right in turn. The VGND line is input to the inverter, and the output of the inverter is the STOP signal connecting to the EN signal of the latch. When the VGND voltage rises sufficiently and the voltage of the STOP signal falls sufficiently, the output value of the latches are fixed. For the waveforms of the proposed temperature sensor at 20°C in shown Fig.12, the latch outputs Q0-Q16 become logic 1 whereas Q17-Q63 are logic 0. This means that the logic value 1 was transmitted through 17 buffer stages before the falling of the STOP signal. At 25°C shown in Figure 13, the outputs Q0-Q14 are logic 1, meaning that the logic value 1 was transmitted through 15 buffer stages. Since the VGND is charged up faster at 25°C than 20°C, the STOP signal falls earlier. This demonstrates that the number of 1`s in the latch outputs Q0-Q63 reflects the temperature.

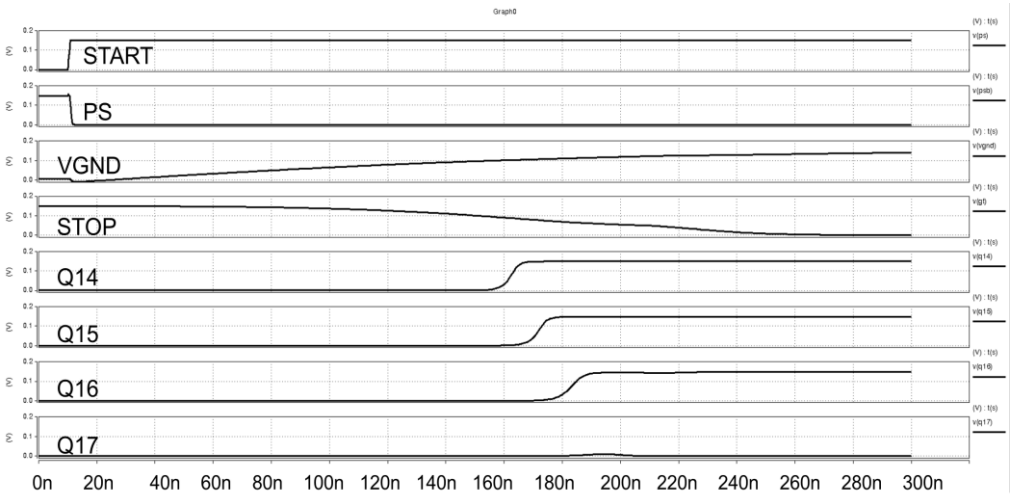

Figure 12. The waveform of the proposed temperature sensor at the 20°C

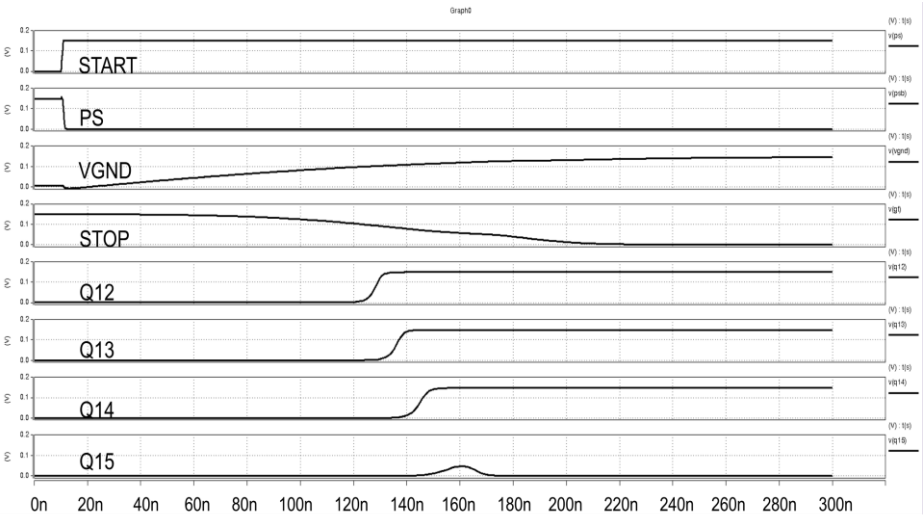

Figure 13. The waveform of the proposed temperature sensor at the 25°C

3.2. Power Consumption

Fig.14 shows the power consumption of the previous and proposed temperature sensors. Compared to the previous temperature sensor, the proposed temperature sensor reduced power consumption to about 1/10 at the maximum. While the power of the previous temperature sensor increased only about 1.5 times as the temperature increased, the power of the proposed temperature sensor increased more than 20 times and exceeded the previous temperature sensor after 80°C. We analysed this reasons.

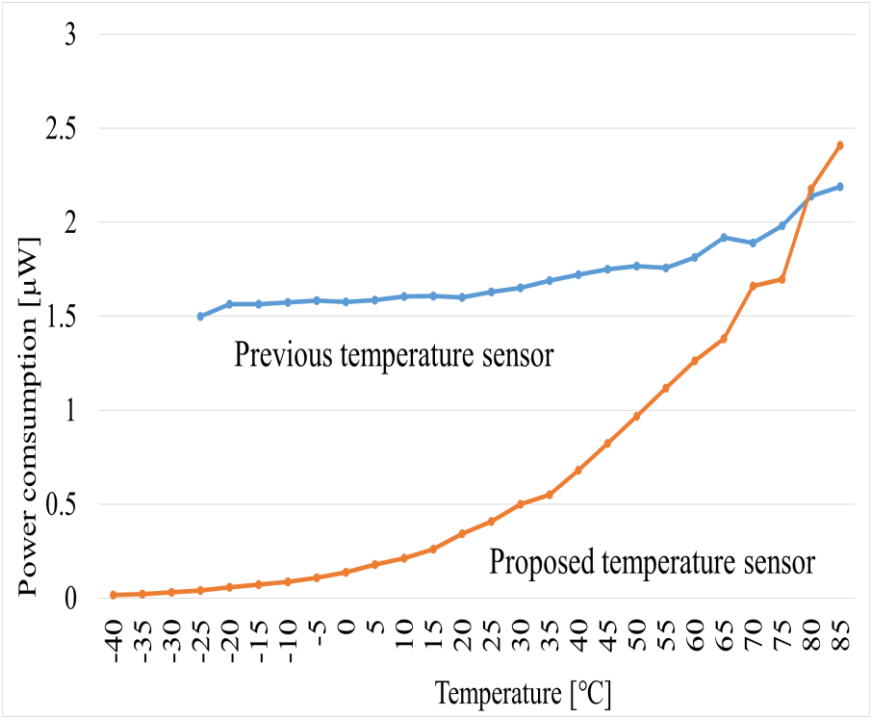

Figure 14. Power Consumption of the Previous and Proposed Temperature Sensors as a function of Temperature

Fig.15 shows the breakdown of the power consumption in the circuit of the previous and the proposed temperature sensors. The loft bar for each temperature shows the power of the previous temperature sensor. In the previous temperature sensor, as the temperature increases, the share of dynamic power decreases and the share of leakage power increases. We think that the reason for the decrease in dynamic power is due to the number of toggles of the flip-flops that make up the counter circuit. Under high temperature conditions, the leakage current increases and the VGND voltage is raised faster, shortening the time it takes to stop the count up. This leads to the reduction of flip-flop toggles. Conversely, under low temperature conditions, the leakage current decreases, the toggle count of the flip-flop increases. For example, the counter circuit of the previous temperature sensor has a 9-bit output, and the counter value is 511 at the lowest temperature. At this time, the flip-flop has toggled a total of 1013 times. At the highest temperature, counter value is 4 and the flip-flop has toggled totally 11 times. This decreases the share of dynamic power as the temperature is elevated. In additionally, we think the reason for the increase in the leakage power ratio is that the leakage current has the characteristic of increasing exponentially with temperature, which has a greater impact.

The power consumption of the proposed temperature sensor shown by the bar on the right shows a significant increase in power with the temperature, with the leakage power accounting for the majority of the total power. The proposed temperature sensor has a 64-bit output, but it toggles only 64 times at most. However, the proposed circuit has 64 buffers and latches, which means that the total size of the gate width of the transistor increases, and the effect of leakage current is large. For these reasons, we think that the effect of leakage power exceeds the effect of dynamic power under high temperature conditions, and the proposed circuit consumes more power than the previous circuit at higher than 85℃.

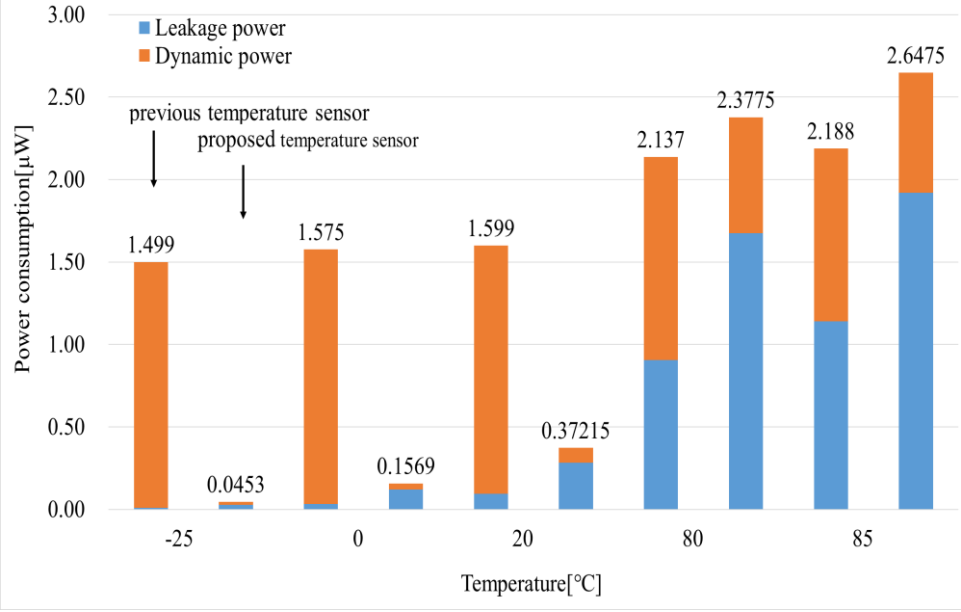

Figure 15. Power Consumption Breakdown of the previous temperature sensor

3.3. Sensing time

Fig.16 shows a comparison of the sensing times of the proposed and the previous temperature sensors. The sensing time is defined as the interval from the START changing to 1 to the STOP changing to 0. The sensing time was shorter in all temperature ranges in the proposed sensor than that of the previous sensor. In the previous circuit, the VGND voltage is input to the Voltage

Comparator and is designed to have a large wiring capacitance. Due to this, the VGND voltage rises slowly to reach the reference voltage, so that the output value of the counter becomes larger at each temperature. In the proposed circuit, the VGND voltage is input to the inverter, and no special circuit design is used to increase the wiring capacitance. This is thought to have shortened the sensing time by reducing the charging time of the VGND voltage compared to the preceding circuit. The fact that the inverter switch voltage is lower than the reference voltage of the Voltage Comparator is also thought to be the reason for the shorter charging time and shorter sensing time. Furthermore, the number of pMOS transistors that charges the VGND voltage is also less in the previous circuit, which could also be the cause.

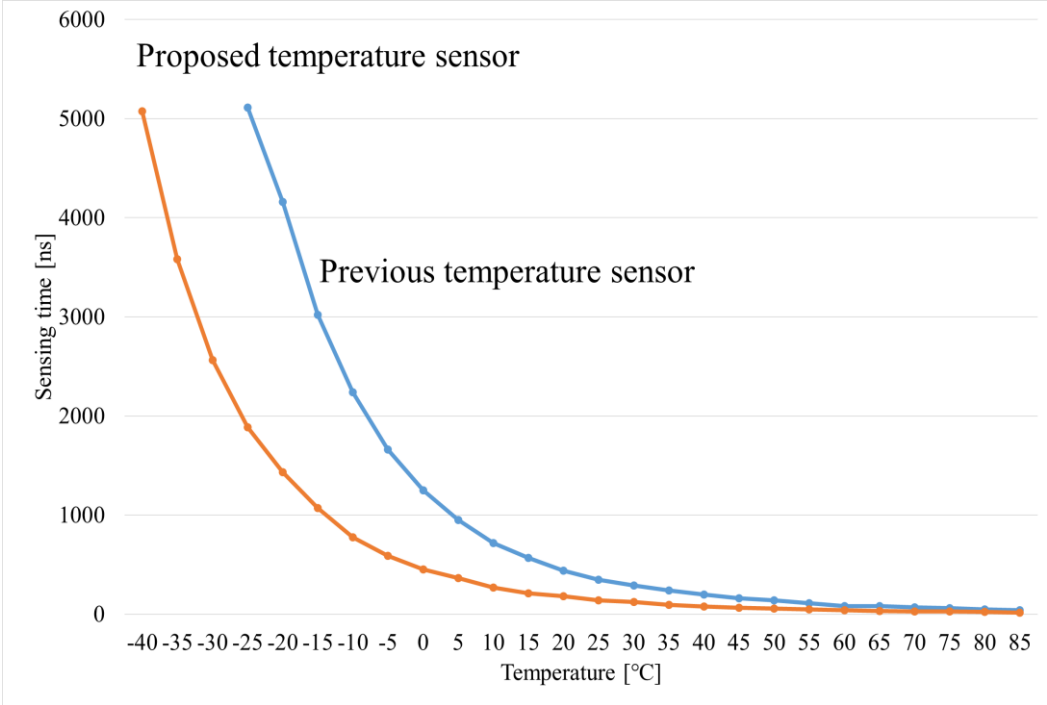

Figure 16. Sensing times of the Previous and Proposed Temperature Sensors

3.4. Energy Consumption

Fig.17 shows a comparison of the energy consumption of the proposed and the previous temperature sensors. The proposed temperature sensor consumed less energy than the previous temperature sensor in all temperature ranges. This is because both power consumption and sensing time are smaller than previous temperature sensors in the -25°C to 75°C range. At the temperature higher than 80°C, the power consumption of the proposed sensor increases to 1.1X of the previous sensor but the sensing time of the proposed sensor is only one-third of that of the previous sensor. This results in lower energy consumption at the proposed temperature sensor.

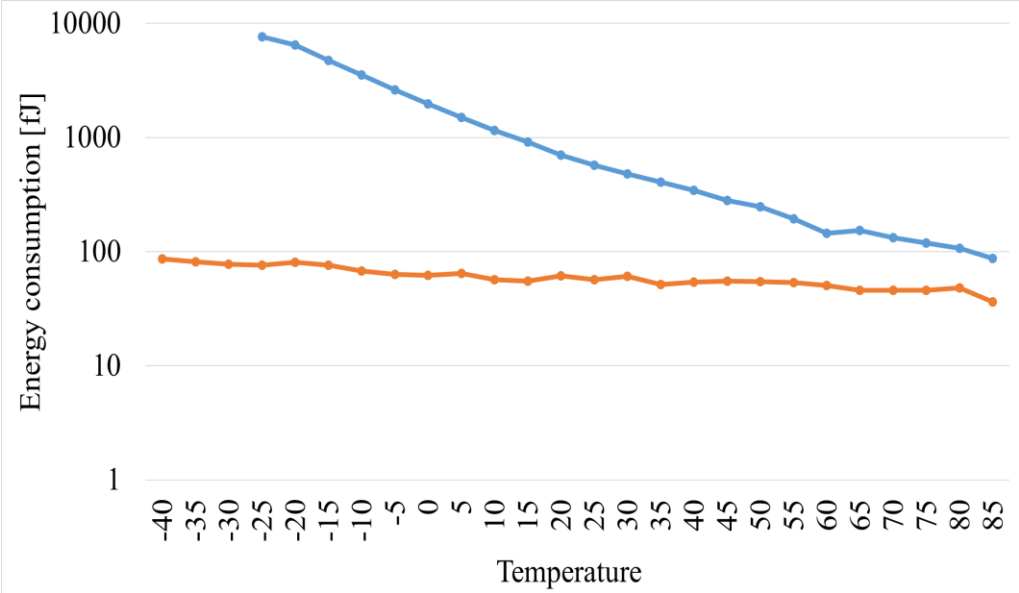

Figure 17. Energy consumption of the Previous and Proposed Temperature Sensors

3.5. Resolution

Fig.18 shows the resolution of the previous and proposed temperature sensors. Resolution is expressed as the ratio of temperature to the output difference. In other words, the upper the value, the finer the accuracy of temperature sensing. As for the resolution, the proposed temperature sensor was not able to exceed the previous sensor in most temperature ranges. We think that this is because the charge time of the VGND voltage was not able to be made longer relative to the buffer delay. As a result, we could not make the output difference larger for the temperature difference.

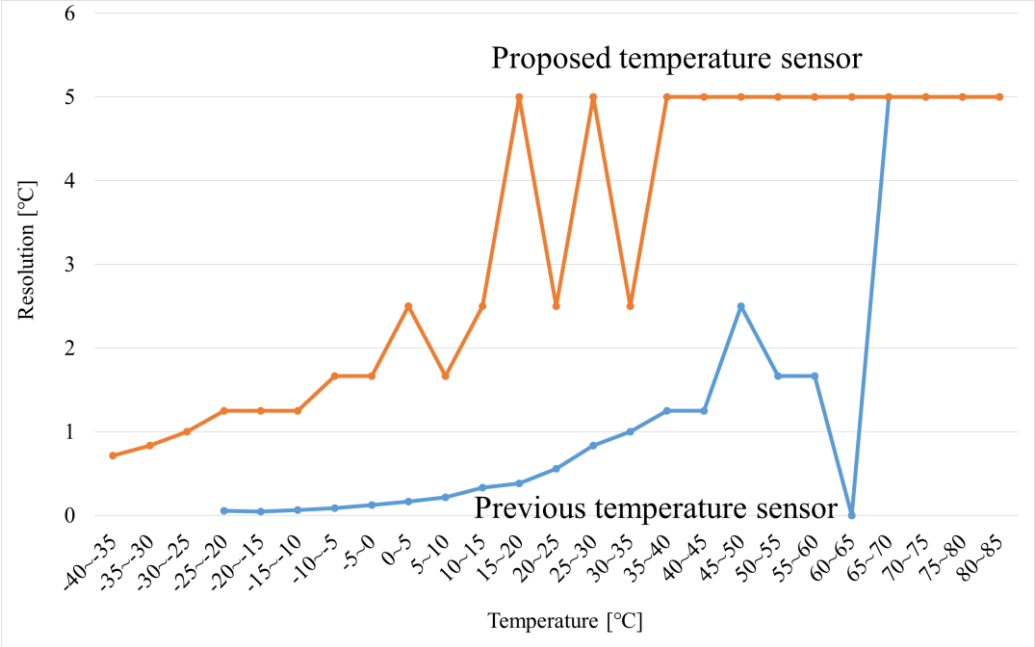

Figure 18. Resolution of the Previous and Proposed Temperature Sensors as a function of Temperature

3.6. Comparison with the previous works

Table.1 compares the proposed temperature sensor of this work with the prior arts. The operating voltage of the proposed temperature sensor of 0.15V is the lowest among the comparative temperature sensors. Regarding the sensing time, the longest time is 5μs in low temperature, but it is shorter in comparison. At the lowest power consumption, the results were below all previous temperature sensors, and even at the highest, the results were quite low. The reduction was as much as 1/100 of that of the previously reported sensors. A comparison of energy consumption showed the lowest energy consumption in all temperature ranges, down to about 1/70. However, the resolution comparison resulted in the lowest performance of all previous temperature sensors.

Table.1 Comparison with the previous works

	this work	IEICE'15[8]	TCAS'22[3]	APCCAS'14[6]	S3S'[7]
Process technology	SOTB 65nm	SOTB 65nm	65nm	350nm	130nm
Minimum supply voltage (V)	0.15	0.2	0.6	1.4	0.2
Sensing Time [min,max]	[20ns,5μs]	[40ns,5μs]	10μs	1.16ms	10ms
Power consumption (μW)	[0.01,2.4]	[1.5,2.2]	47	3.5	0.023
Energy consumption	[63fJ,101fJ]	[90fj,7700fJ]	472pJ	-	230pJ
Resolution (℃)	[0.7,5]	[0.05,5]	0.12	0.3	0.008
Temp. range (℃)	[-40,85]	[-25,85]	[-45,85]	[-40,125]	[0,100]

*Sensing time changes depending on the temperature in the first two sensors.
*The data in the second column are the values derived from my own simulation.

4. CONCLUSION

In this paper, we proposed a temperature sensor using the buffer-chain based TDC circuit. Simulation results demonstrated that the proposed temperature sensor operates at the supply voltage 0.15V. The measurable range of temperature was found to be -45°C to 85°C. By replacing the counter circuit that were responsible for most of the power consumption, the proposed circuit was able to significantly reduce power consumption. Furthermore, sensing time was reduced in all temperature ranges. Significant reductions in power consumption and sensing time have also significantly reduced energy consumption. However, resolution has been low at all temperature ranges.

As the future work, we will improve resolution and implement a test chip to conduct actual measurements. Also we will study reliability issues including aging of the proposed temperature sensor.

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