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Exploring Transimpedance Amplifier Topologies: Design Considerations and Trade-offs

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ABSTRACT. Transimpedance amplifiers (TIAs) are crucial in converting current signals from sensors, photodiodes, and other transducers into voltage signals for processing in various electronic systems. This paper explores three TIA topologies: common emitter with negative resistive feedback, regulated cascode, and Darlington pair with negative resistive feedback. Each topology offers unique advantages and trade-offs regarding bandwidth, gain, and noise performance. We analyze the characteristics of each topology, discussing their impact on TIA design and performance. We investigate methods to optimize gain, bandwidth, and noise performance for different application requirements through theoretical analysis and circuit simulations. Our findings provide valuable insights into TIA design considerations, offering engineers a comprehensive understanding of TIA topologies and their implications for electronic system design.

KEYWORDS: Common Base, Common Emitter, Regulated Cascode, Darlington Pair, Optical receivers, SiGe BiCMOS technology, Transimpedance Amplifier

1 INTRODUCTION

The communications sector's evolution, driven by multimedia technologies, has underscored the importance of high-speed data transfer. Conventional electronic communication faces challenges such as limited bandwidth, crosstalk, and susceptibility to interference. In response, fiber optic cables have emerged as a high-bandwidth alternative, revolutionizing global data transmission [1][2]. Optical fiber technology, pioneered by GTE and AT&T in 1977, has since dominated long-distance communication, boasting minimal signal loss, resistance to interference, and terabit-per-second transmission capabilities over vast distances [3].

At the forefront of optical communication systems, the transimpedance amplifier (TIA) plays a pivotal role. As the first stage after the photodiode, the TIA converts electrical current to voltage with minimal noise and adequate bandwidth. Achieving a high signal-to-noise ratio (SNR) and mitigating intersymbol interference (ISI) is paramount, making the TIA the cornerstone of optical receivers [4].

Designing an effective TIA entails balancing numerous factors, including noise, bandwidth, gain, and stability. The TIA's low input impedance, necessary for interfacing with the photodiode, and its ability to convert input current to voltage demand careful consideration of topology. With diverse requirements in mind, selecting the optimal TIA topology becomes imperative.

Four distinct topologies—common base, common emitter with resistive feedback, regulated cascode, and Darlington pair with resistive feedback—offer varying trade-offs in performance. Our objective in this paper is to identify the topology that best aligns with the desired TIA performance criteria.

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2 TRANSIMPEDANCE AMPLIFIER TOPOLOGIES

In optical communication systems, the transimpedance amplifier (TIA) serves a critical role by converting the low current generated by photodiodes into voltage. A straightforward approach involves using a single resistor to achieve this conversion, albeit with significant trade-offs between gain, bandwidth, and noise. The transimpedance gain of such a resistor-based TIA, expressed in terms of impedance and decibels per ohm, is given by Equations 1 and 2.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{R_L}{1 + j2\pi f R_L C_T} \quad \Omega \tag{1}$$

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = 20log\left(\frac{R_L}{1 + j2\pi f R_L C_T}\right) dB\Omega \tag{2}$$

Where f represents frequency, and $C_T = C_{PD} + C_L$ denotes the total capacitance comprising photodiode and load capacitances, with C_L typically smaller than C_{PD}. The DC transimpedance gain, is approximately equal to R_L, while the bandwidth of the TIA is given by Equation 3.

$$BW_{TIA} = \frac{1}{2\pi R_L C_T} \quad Hz \tag{3}$$

To assess input-referred noise, considerations must include contributions from R_L,C_L,and C_{PD}. The output noise voltage power spectral density (PSD) ($\overline{V_{n,out}^2}$) can be derived, as shown in Equation 4, considering noise from R_L and the equivalent output resistance R_{out}.

$$\begin{aligned} \overline{V_{n,out}^2} &= \int_0^\infty \overline{I_{n,R_L}{}^2} |R_{out}|^2 \, df \\ &= \int_0^\infty \frac{4kT}{R_L} \frac{R_L^2}{R_L^2 C_{PD}^2 4\pi^2 f^2 + 1} \, df \\ &= \frac{kT}{C_{PD}} \quad \frac{V^2}{Hz} \end{aligned} \tag{4}$$

Here, $\overline{I_{n,R_L}{}^2}$ represents noise from the resistance, with R_{out} indicating the equivalent output resistance. Consequently, the input-referred noise current PSD ($\overline{I^2{}_{n,in}}$) is expressed in Equation 5.

$$\overline{I^2{}_{n,in}} = \frac{kT}{R_L^2 C_{PD}} \quad \frac{A^2}{Hz} \tag{5}$$

While increasing R_L enhances gain and reduces input noise, it leads to bandwidth reduction. Hence, leveraging more complex structures is imperative to balance these design parameters effectively.

2.1 COMMON BASE TIA

The common-base (CB) topology, known for its low input impedance and high bandwidth, has been a staple in wideband optical communication systems since the 1980s. This architecture offers high voltage gain and output impedance, desirable characteristics in TIA design. Despite its advantages, CB TIAs tend to exhibit higher noise levels due to the direct addition of transistor noise to the input signal. Figure 1 illustrates a typical CB TIA

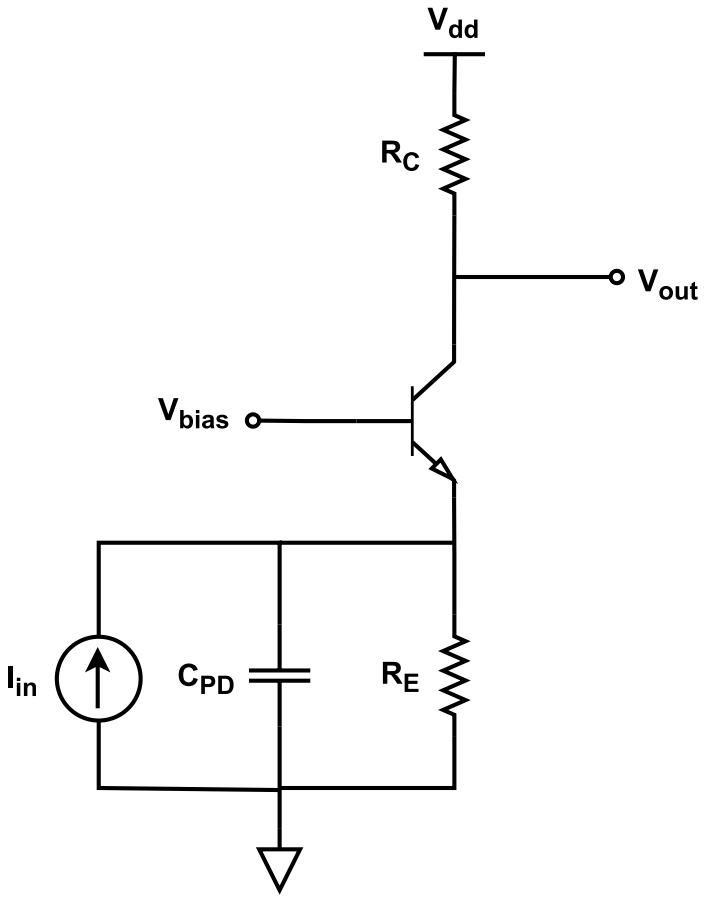

Figure 1. Circuit diagram of a basic common base TIA.

configuration, featuring a transistor biased at the base with voltage V_{bias} and a resistive load R_C.

The small signal model of a CB amplifier helps analyze its high-frequency response. Input and output capacitances (C_{in} and C_{out}) comprise photodiode and internal transistor capacitances, while R_E, r_π, and g_m represent emitter resistance, internal base-emitter resistance, and transistor transconductance, respectively.

By neglecting early effect and base resistance, the CB TIA gain function is represented by equation 6, simplifies when r_b is small and transistor current gain β is large. Consequently, the DC transimpedance gain is approximately equal to R_C.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{g_m R_C}{(g_m + sC_{in})(sR_C C_{out} + 1)} \quad \Omega \tag{6}$$

The CB TIA exhibits an input impedance close to $\frac{1}{g_m}$, with input capacitances C_{in} decoupled from the output. Thus, its broadband bandwidth allows for flexible gain, bandwidth, and noise trade-offs. Equation 7 highlights two dominant poles p_1 at the input and p_2 at the output governing the CB TIA's bandwidth.

$$\begin{aligned} p_1 &= \frac{1}{2\pi \frac{1}{g_m} C_{in}} \quad Hz \\ p_2 &= \frac{1}{2\pi R_C C_{out}} \quad Hz \end{aligned} \tag{7}$$

The total input-referred noise current PSD, represented in Equation 8, combines thermal noise from resistors and transistor base, along with short noise contributions. Increasing R_C enhances gain but reduces available voltage headroom and bandwidth due to decreased p_2 pole frequency. Conversely, reducing R_C lowers gain and increases input-referred noise due to thermal noise. Managing noise sources like $\overline{I^2{}_{n,I_C}}$ and $\overline{I^2{}_{n,r_b}}$ is crucial for optimal noise performance.

$$\begin{aligned}\overline{I^2{}_{n,TIA}}(f^2) = &\frac{4kT}{R_C} + \frac{4kT}{R_E} + \frac{2qI_C}{\beta} \\ &+ 2qI_C\frac{(2\pi C_{in})^2}{{g_m}^2}f^2 + 4kTr_b(2\pi C_{PD})^2 f^2 \ \frac{A^2}{Hz}\end{aligned} \tag{8}$$

2.2 COMMON EMITTER WITH NEGATIVE RESISTIVE FEEDBACK TIA

The shunt-feedback TIA topology, depicted in Figure 2, is prevalent in optical fiber applications due to its high current and voltage gain, along with sufficient bandwidth. However, maintaining stability across temperature variations requires sophisticated bias networks and emitter degeneration. While the common-emitter (CE) topology typically offers high input impedance, shunt-shunt feedback is often employed in TIA design to lower input impedance and reduce noise. Additionally, the Miller effect can impede the CE stage's bandwidth.

Under the condition of large transistor current gain ($\beta >> 1$) and small base resistance (r_b), the transimpedance gain function of the CE TIA with resistive feedback is expressed in Equation 9. The DC transimpedance gain is approximately $(R_C||R_F)$.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{g_m(R_C||R_F)}{(1 + s(R_C||R_F)C_{out})} \quad \Omega \tag{9}$$

The CE TIA exhibits an input impedance of $\frac{R_F}{1+sR_FC_{in}}$ and output impedance of $\frac{(R_C||R_F)}{1+s(R_C||R_F)C_{out}}$. By utilizing feedback resistor R_F, CE TIA effectively isolates input capacitances C_{in} from the output, facilitating flexible gain, bandwidth, and noise trade-offs. The circuit's bandwidth is determined by dominant poles p_1 and p_2, as shown in Equation 10.

$$\begin{aligned}p_1 &= \frac{1}{2\pi R_F C_{in}} \quad Hz \\ p_2 &= \frac{1}{2\pi(R_C||R_F)C_{out}} \quad Hz\end{aligned} \tag{10}$$

Noise contributions from various sources are consolidated into an equivalent noise current source $\overline{I^2{}_{n,in}}$ at the input, as detailed in Equation 11. Adjusting $R_C||R_F$ impacts gain and voltage headroom while modifying R_C and R_F influences bandwidth and input-referred noise. Optimal trade-offs between gain, bandwidth, and noise are achieved by selecting suitable values for these resistors.

$$\begin{aligned}\overline{I^2{}_{n,TIA}}(f^2) = &\frac{4kT}{R_C} + \frac{4kT}{R_F} + \frac{2qI_C}{\beta} \\ &+ 2qI_C\frac{(2\pi C_{in})^2}{{g_m}^2}f^2 + 4kTr_b(2\pi C_{PD})^2 f^2 \quad \frac{A^2}{Hz}\end{aligned} \tag{11}$$

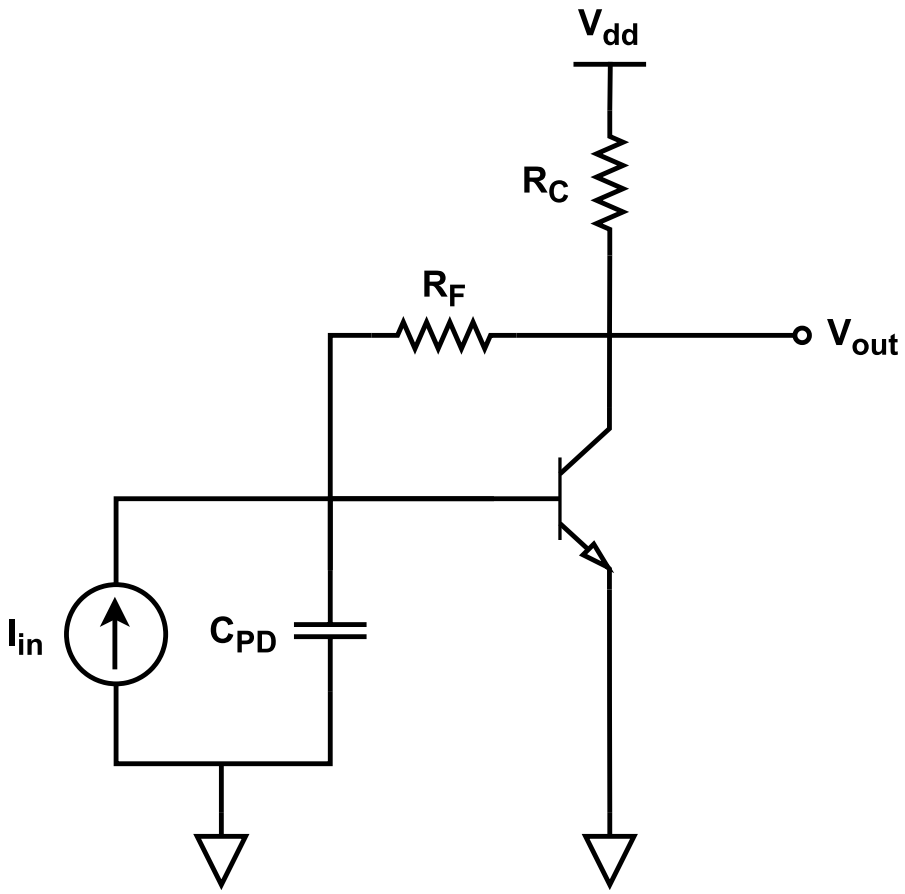

Figure 2. Circuit diagram of a basic common emitter TIA.

2.3 REGULATED CASCODE TIA

To alleviate the stringent trade-offs observed in common-base topology, the regulated cascode (RGC) TIA, depicted in Figure 3, is commonly employed. This two-stage shunt-series feedback amplifier offers enhanced bandwidth, noise performance, and gain flexibility. The RGC TIA can be conceptualized in two ways: as a common-base transistor with local feedback, or as a closed-loop current amplifier comprising two common-emitter stages encircled by shunt-series resistive feedback.

Under the assumption of large transistor current gains ($\beta_1, \beta_2 >> 1$) and small base resistances ($r_{b_1}, r_{b_2} << 1$), the transimpedance gain function of the RGC TIA is given by Equation 12. The DC transimpedance gain is approximately R_{C_2}.

$$Z_{TIA} = \frac{V_{out}}{I_{in}} = \frac{R_{C_2}(1 + sR_{C_1}C_{out})}{(1 - sR_{C_1}R_{C_2}C_{\mu_2})} \quad \Omega \tag{12}$$

Analysis of input and output impedances reveals crucial poles and zeros dictating the circuit's bandwidth. Equation 13 elucidates input impedance, pole, and zero, while Equation 14 delineates output impedance, pole, and zero. Adjusting R_{C_2} and R_E can cancel input pole and zero frequencies, enhancing bandwidth. However, increasing R_{C_2} reduces voltage headroom, while lowering R_{C_1} improves bandwidth but complicates gain prediction due to changes in output pole frequency.

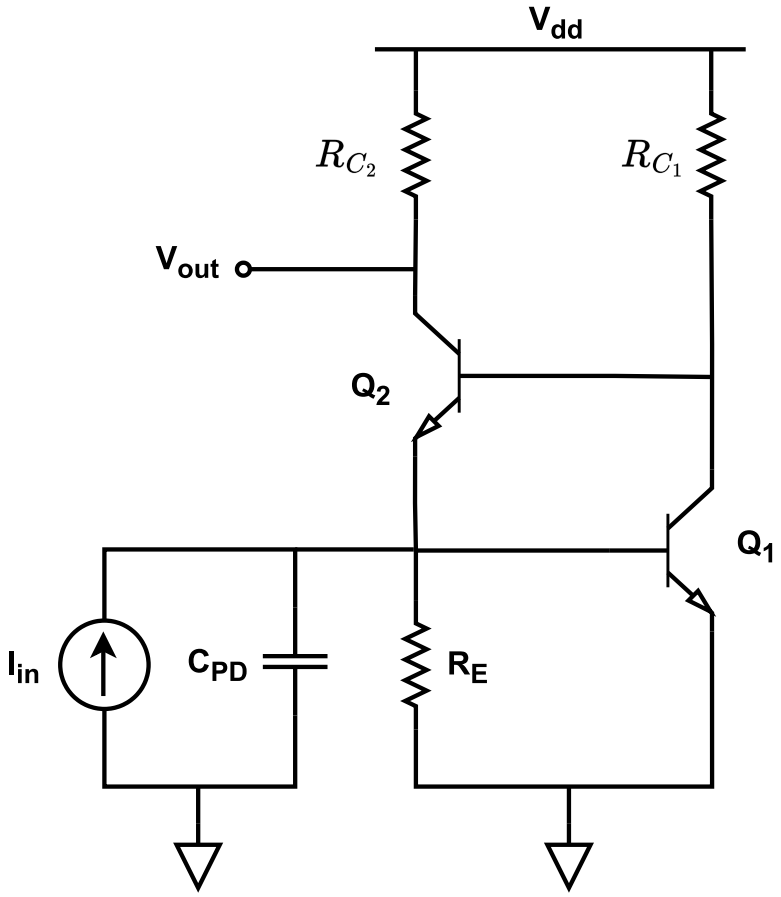

Figure 3. Circuit diagram of a basic regulated cascode TIA.

$$
\begin{aligned}
Z_{in} = \frac{V_{in}}{I_{in}} = (R_{C_2} + R_E)\frac{1 + s(R_{C_2}||R_E)C_{in}}{1 + sR_EC_{in}} \quad & \Omega \\
p_1 = \frac{1}{2\pi R_EC_{in}} \quad & Hz \\
z_1 = \frac{1}{2\pi(R_{C_2}||R_E)C_{in}} \quad & Hz
\end{aligned}
\tag{13}
$$

$$
\begin{aligned}
Z_{out} = \frac{V_{out}}{I_{out}} = \frac{1 + sR_{C_1}C_{out}}{1 + s(R_{C_1}C_{out} + R_{C_2}C_{\pi_2})} \quad & \Omega \\
p_2 = \frac{1}{2\pi(R_{C_1}C_{out} + R_{C_2}C_{\pi_2})} \quad & Hz \\
z_2 = \frac{1}{2\pi R_{C_1}C_{out}} \quad & Hz
\end{aligned}
\tag{14}
$$

The total input-referred noise current, described by Equation 15, incorporates thermal noise from collector and degenerative emitter resistors, as well as short noise from collector currents. Balancing RGC TIA gain, bandwidth, and input-referred noise requires a careful selection of resistor values.

$$\begin{aligned}\overline{I^2{}_{n,TIA}}(f^2) = &\frac{4kT}{R_{C_1}} + \frac{4kT}{R_{C_2}} + \frac{4kT}{R_E} \\ &+ 2qI_{C_1}\frac{(2\pi C_{in})^2}{{g_{m_1}}^2}f^2 + 2qI_{C_2}\frac{(2\pi C_{in})^2}{{g_{m_2}}^2}f^2 \quad \frac{A^2}{Hz}\end{aligned} \tag{15}$$

In summary, optimizing the RGC TIA for transimpedance gain, bandwidth, and input-referred noise entails intricate trade-offs, necessitating meticulous resistor adjustments to achieve desired performance metrics.

2.4 DARLINGTON PAIR WITH NEGATIVE RESISTIVE FEEDBACK TIA

To address the limitations of the common-emitter topology, a Darlington pair with negative resistive feedback presents an alternative approach. This configuration capitalizes on the high current gain provided by a Darlington pair while mitigating its inherent high input impedance through negative feedback. The Darlington pair, composed of two bipolar transistors, offers significantly amplified current gain from a low base current, enhancing overall circuit performance [5].

In the schematic depicted in Figure 4, the incoming current signal is initially amplified by transistor Q_1 with a current gain factor of β_1. The resulting emitter current from Q_1 is then further amplified by transistor Q_2 with a gain factor of β_2, effectively combining their gains. This Darlington pair TIA topology resembles a single common-emitter TIA but with substantially higher current gain.

The DC transimpedance gain $Z_{TIA_{DC}}$ of the Darlington pair TIA can be determined by separately calculating the DC gains of the constituent transistors Q_1 and Q_2 and multiplying them, as shown in Equation 16.

$$Z_{TIA_{DC}} = \frac{V_{out}}{I_{in}} \approx \beta_1 R_E g_{m_2}(R_C||R_F) \quad \Omega \tag{16}$$

The bandwidth of the Darlington pair TIA is influenced by the dominant poles at the input and output, as illustrated in Equation 17. Adjusting parameters such as R_E, R_C, and R_F allows for a trade-off between TIA gain and bandwidth.

$$\begin{aligned}p_1 &= \frac{1}{2\pi\beta_1 R_E C_{in}} \quad Hz \\ p_2 &= \frac{1}{2\pi(R_C||R_F)C_{out}} \quad Hz\end{aligned} \tag{17}$$

Analyzing the total input-referred noise current in Equation 18 provides insights into the interplay between gain, bandwidth, and noise. Balancing these factors requires careful selection of resistor values to optimize TIA performance.

$$\begin{aligned}\overline{I^2{}_{n,TIA}}(f^2) = &\frac{4kT}{R_F} + \frac{4kT}{R_C} + \frac{4kT}{R_E} \\ &+ \frac{2qI_{C_{eff}}}{\beta_1\beta_2} + 2qI_{C_{eff}}\frac{(2\pi C_{in})^2}{{g_{m_2}}^2}f^2 \quad \frac{A^2}{Hz}\end{aligned} \tag{18}$$

In summary, optimizing the Darlington pair TIA with negative resistive feedback entails adjusting parameters to achieve desired gain, bandwidth, and noise performance, thereby offering flexibility in TIA design.

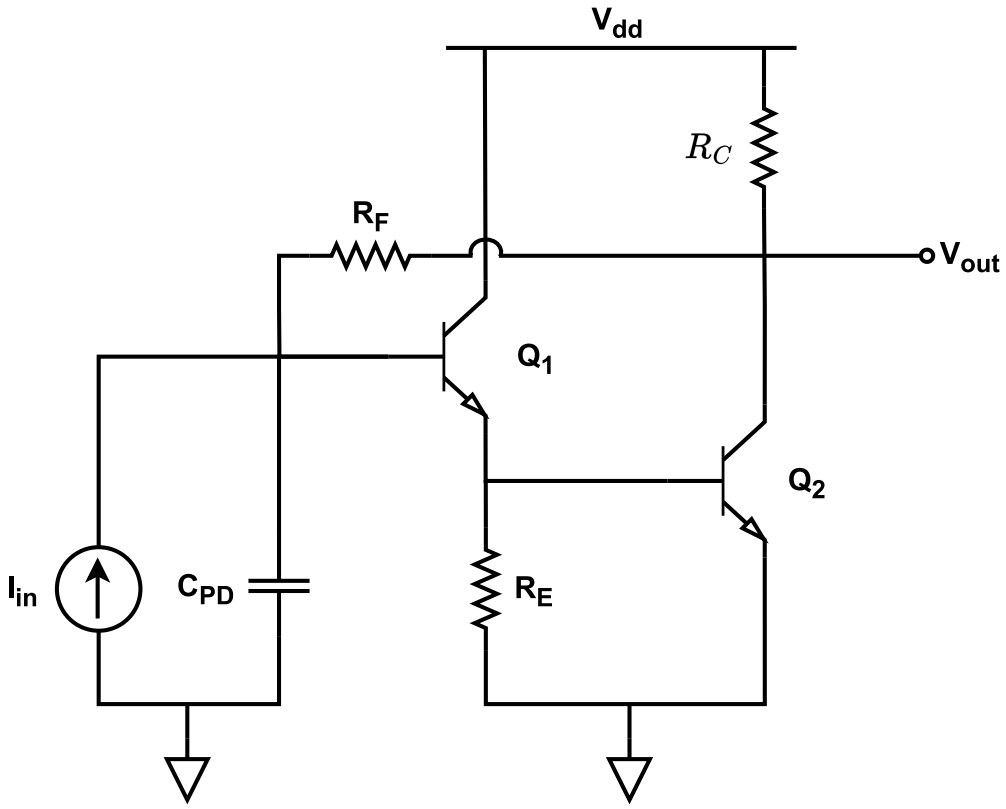

Figure 4. Circuit diagram of a basic Darlington TIA with Negative Resistive Feedback.

3 DISCUSSION

A summarized table 1 compares performance parameters for different TIA topologies discussed above. In designing the preferred TIA for an optical communication system, selecting the appropriate topology is critical to achieving the desired balance between gain, bandwidth, and noise performance.

The CB topology, with its simple design, offers a relatively high bandwidth due to its low input capacitance. The primary advantage of the CB topology lies in its simplicity and high-speed performance, making it suitable for applications where bandwidth is a critical factor. However, this simplicity comes at the cost of higher noise contributions from the base resistance and the emitter resistor R_E. Additionally, the gain of the CB topology is directly dependent on R_C, limiting the achievable gain without compromising the bandwidth.

The CE RSF topology improves upon the CB design by introducing a feedback resistor R_F, which enhances the gain. This topology strikes a reasonable balance between gain and noise performance. The feedback resistor helps in stabilizing the gain, but it also introduces a trade-off where the bandwidth might be slightly reduced compared to the CB topology. Nonetheless, the CE RSF topology is favored for its balanced performance and reasonable complexity, making it a versatile choice for many applications.

The RGC topology is known for its high gain and bandwidth, achieved through its cascode configuration. This design offers excellent isolation between the input and output, enhancing stability and making it suitable for high-performance applications. However, the complexity of the RGC topology is higher than that of the CB and CE RSF topologies. The increased number of active devices in the RGC design can lead to higher noise and power

Table 1. Comparison of performance parameters for different TIA topologies.

	TIA DC Gain (Ω)	**Poles & Zeros** (Hz)	**IRN** (A^2/Hz)
CB	R_C	$p_1 = \frac{1}{2\pi \frac{1}{g_m} C_{in}}$, $p_2 = \frac{1}{2\pi R_C C_{out}}$	$\frac{4kT}{R_C} + \frac{4kT}{R_E} + \frac{2qI_C}{\beta} + 2qI_C \frac{(2\pi C_{in})^2}{{g_m}^2} f^2 + 4kTr_b(2\pi C_{PD})^2 f^2$
CE RSF	$(R_C \| R_F)$	$p_1 = \frac{1}{2\pi R_F C_{in}}$, $p_2 = \frac{1}{2\pi (R_C \| R_F) C_{out}}$	$\frac{4kT}{R_C} + \frac{4kT}{R_F} + \frac{2qI_C}{\beta} + 2qI_C \frac{(2\pi C_{in})^2}{{g_m}^2} f^2 + 4kTr_b(2\pi C_{PD})^2 f^2$
RGC	R_{C_2}	$p_1 = \frac{1}{2\pi R_E C_{in}}$ $z_1 = \frac{1}{2\pi (R_{C_2} \| R_E) C_{in}}$ $p_2 = \frac{1}{2\pi (R_{C_1} C_{out} + R_{C_2} C_{\pi_2})}$ $z_2 = \frac{1}{2\pi R_{C_1} C_{out}}$	$\frac{4kT}{R_{C_1}} + \frac{4kT}{R_{C_2}} + \frac{4kT}{R_E} + 2qI_{C_1} \frac{(2\pi C_{in})^2}{{g_{m_1}}^2} f^2 + 2qI_{C_2} \frac{(2\pi C_{in})^2}{{g_{m_2}}^2} f^2$
DP RSF	$\beta_1 R_E$ $g_{m_2}(R_C \| R_F)$	$p_1 = \frac{1}{2\pi \beta_1 R_E C_{in}}$, $p_2 = \frac{1}{2\pi (R_C \| R_F) C_{out}}$	$\frac{4kT}{R_F} + \frac{4kT}{R_C} + \frac{4kT}{R_E} + \frac{2qI_{C_{eff}}}{\beta_1 \beta_2} + 2qI_{C_{eff}} \frac{(2\pi C_{in})^2}{{g_{m_2}}^2} f^2$

consumption. Despite these drawbacks, the RGC topology is often chosen for applications that demand high gain and bandwidth.

The DP RSF topology provides the highest gain among the four topologies, thanks to its cascaded transistor stages. This design also offers high input impedance and low output impedance, beneficial for various high-speed applications. However, the complexity and power consumption of the DP RSF topology are significantly higher due to the multiple transistors and feedback network. The noise performance may also be compromised due to the increased number of active devices and the potential introduction of multiple poles that can affect the bandwidth.

In summary, the selection of a TIA topology should be guided by the specific requirements of the application. The CB topology is ideal for scenarios where simplicity and high bandwidth are paramount, albeit with a trade-off in noise performance and gain. The CE RSF topology offers a balanced approach, providing reasonable gain and noise performance with moderate complexity. The RGC topology is suitable for applications requiring high gain and bandwidth, though at the cost of increased design complexity and power consumption. Finally, the DP RSF topology is best for applications demanding the highest gain, despite its higher complexity, power consumption, and potential noise issues.

4 CONCLUSION

In this paper, we have explored various topologies of transimpedance amplifiers (TIAs) and their implications on performance parameters such as bandwidth, gain, and noise. Each TIA topology offers distinct advantages and trade-offs, providing engineers with a range of options to tailor amplifier designs to specific application requirements.

The common-emitter TIA, despite its widespread use, presents challenges in balancing gain, bandwidth, and noise due to the inherent trade-offs imposed by its topology. However, incorporating negative resistive feedback in common-emitter TIAs can mitigate some of these limitations, enhancing overall performance.

The Regulated Cascode (RGC) TIA introduces a two-stage shunt-series feedback amplifier, which helps to relax the trade-offs between bandwidth, gain, and noise. This topol-

ogy offers a promising alternative to the common-emitter configuration by providing better isolation between the input and output, which enhances stability.

Furthermore, the Darlington pair with negative resistive feedback presents a unique approach. This topology leverages the high current gain of a Darlington pair while addressing input impedance concerns through negative feedback. It offers flexibility in optimizing gain, bandwidth, and noise performance, making it a valuable option in TIA design.

In conclusion, the selection of a TIA topology depends on specific application requirements and desired performance characteristics. By understanding the trade-offs associated with each topology and carefully tuning circuit parameters, engineers can design TIAs that meet the demands of diverse applications in fields such as optical fiber communication, sensor systems, and instrumentation. This study contributes to the advancement of high-speed optical communication systems by providing insights into effective TIA design that balances performance, efficiency, and simplicity.

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